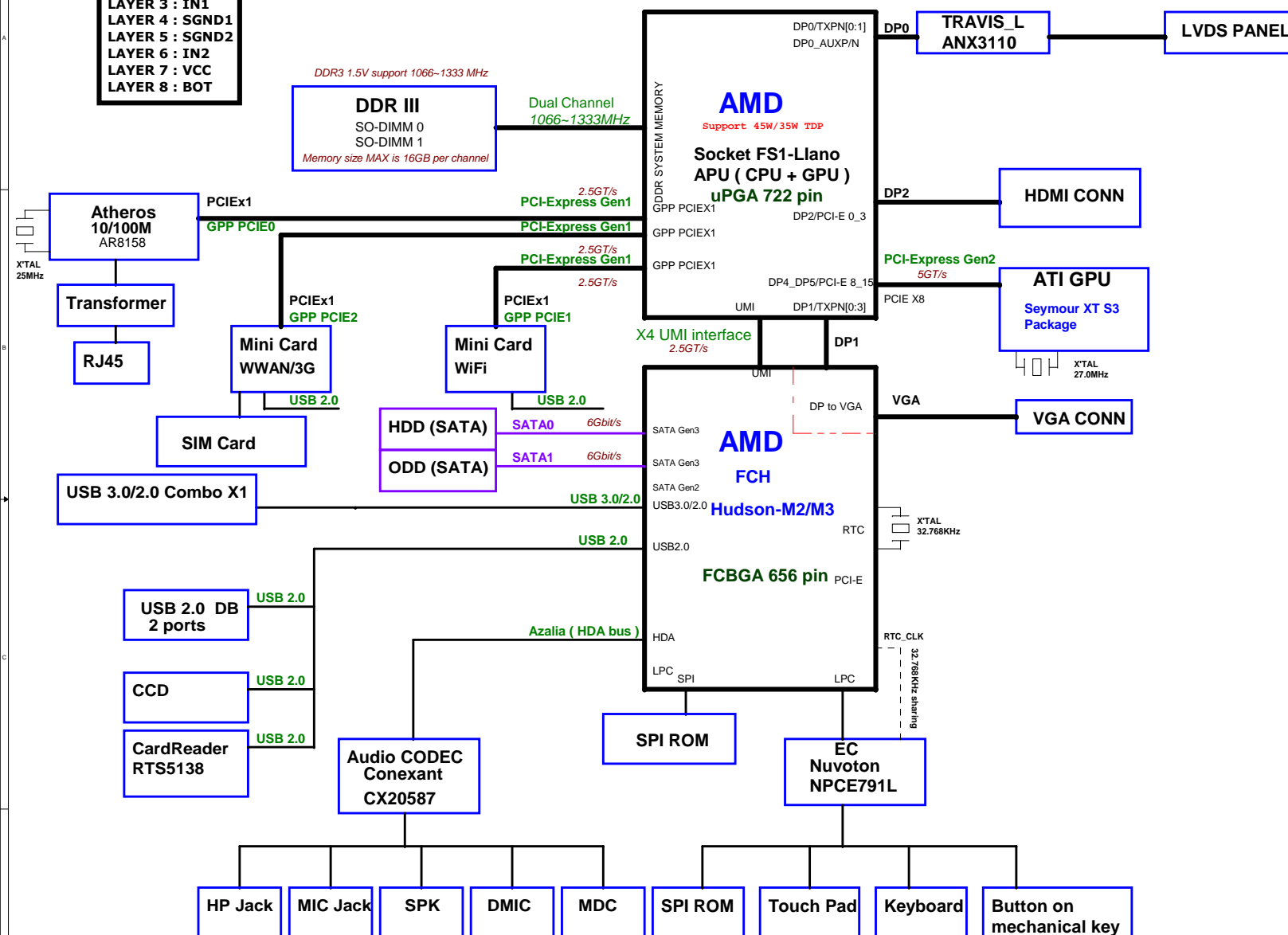


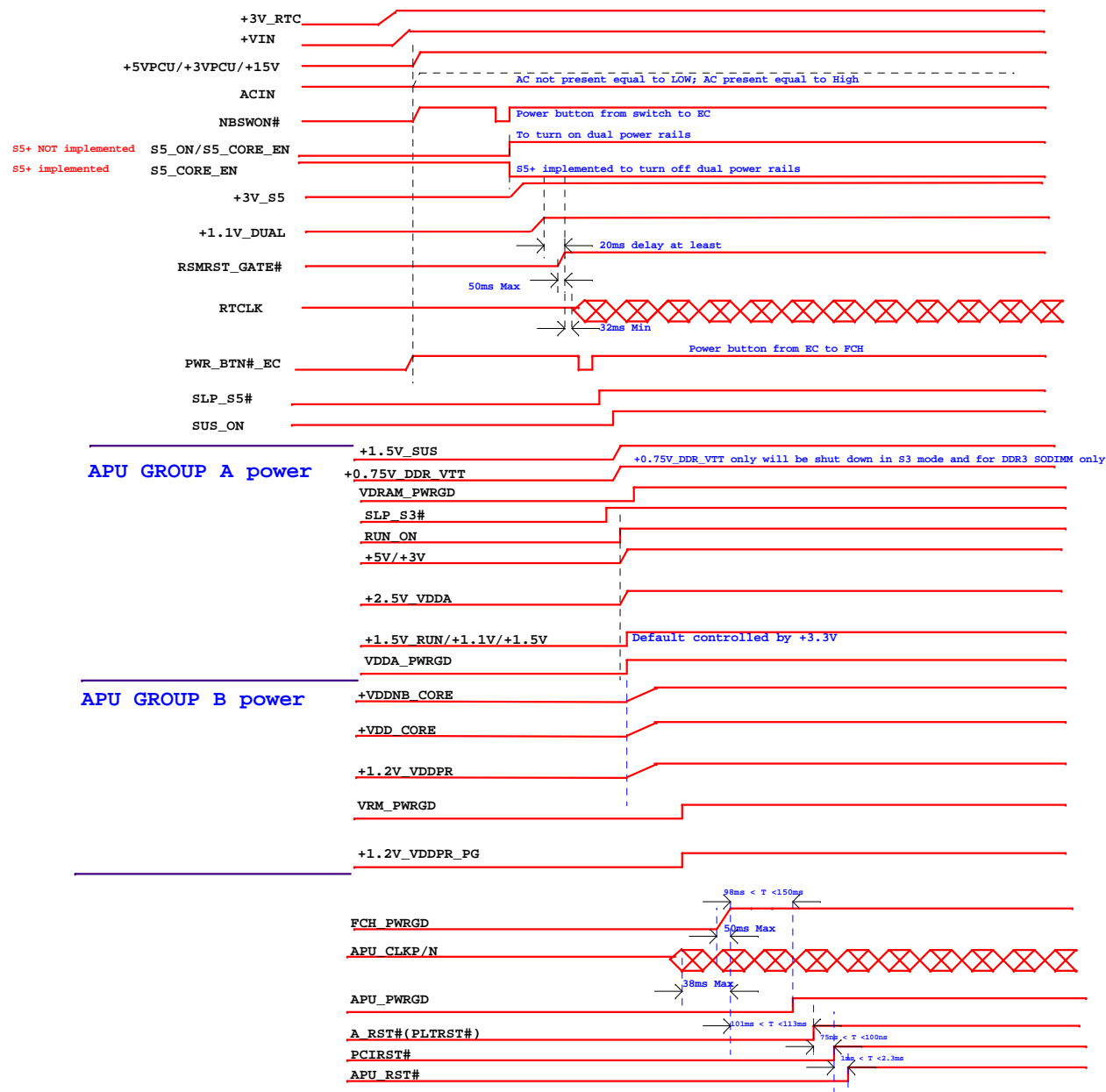
## PCB STACK UP

LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : SGND1  
 LAYER 5 : SGND2  
 LAYER 6 : IN2  
 LAYER 7 : VCC  
 LAYER 8 : BOT

## BLOCK DIAGRAM



## BLF/BLFD Power On Sequence: S5 &gt; S0



## APU Power on sequence required:

## Llano APU:

- 1.Group A ( +1.5V\_SUS, +2.5V\_VDDA ) ramp before Group B ( +VDD\_CORE, +VDDNB\_CORE, +1.2V\_VDDPR )

## HUDSON-M2/M3:

- 1.+3V\_S5 ramp before +1.1V\_DUAL
- 2.+3V ramp before +1.1V
- 3.+3V\_RTC must ramp at least 5 secs before the +3V\_S5

## Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

- 1=> +3V\_GPU
- 2=> +VGPU\_CORE/+1V\_GPU
- 3=> +VGPU\_CORE PWRGD to enable +1.5V\_GPU
- 4=> +1V\_GPU PWRGD to enable +1.8V\_GPU

## NOTE

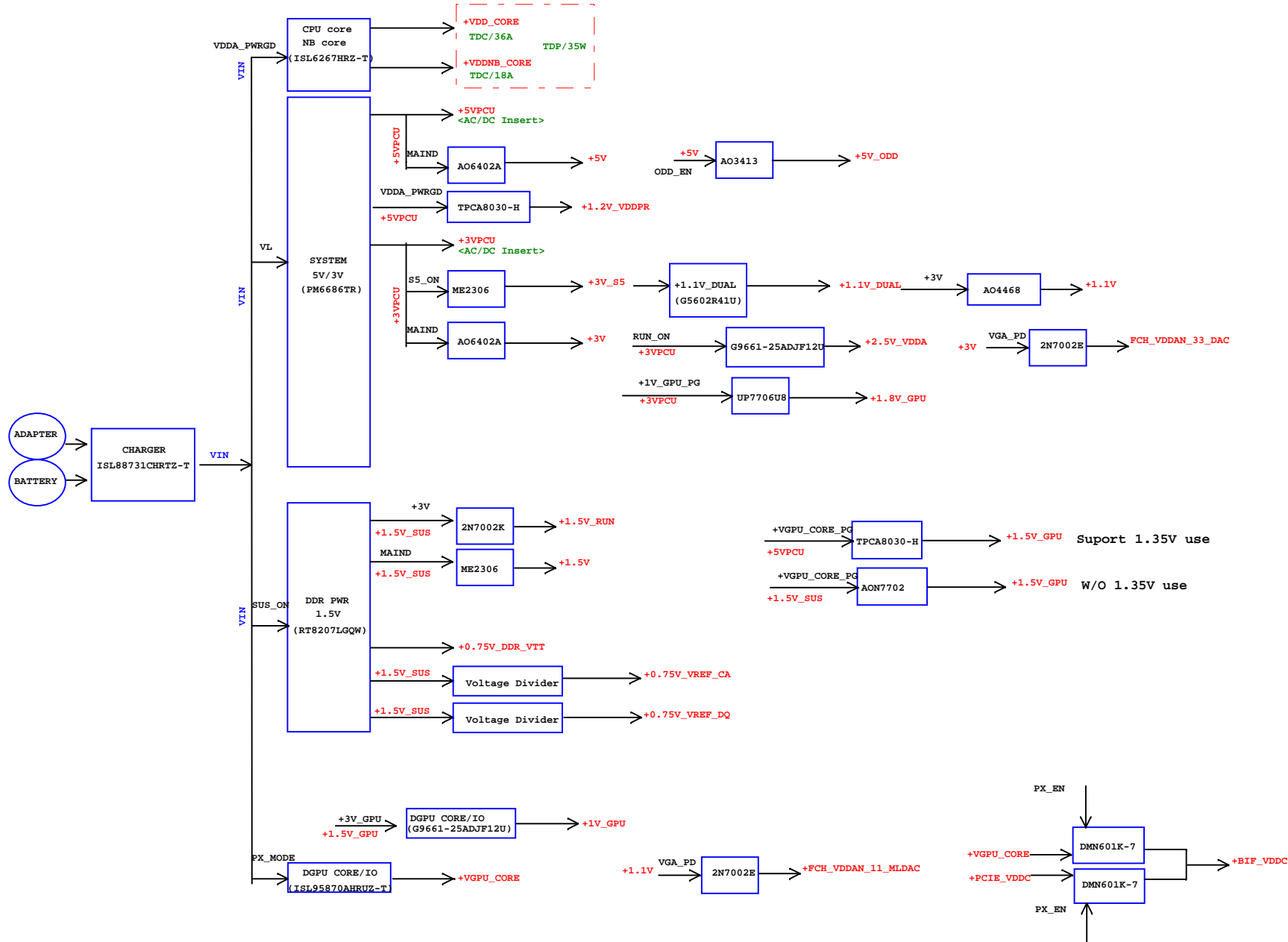
- 1.+3V to turn on +3V\_GPU
- 2.+3V\_GPU ready to enable +VGPU\_CORE/+1V\_GPU ( +1V\_GPU will ramp up before +VGPU\_CORE )
- 3.+VGPU\_CORE PWRGD to enable +1.5V\_GPU
- 3.+1V\_GPU PWRGD to enable +1.8V\_GPU

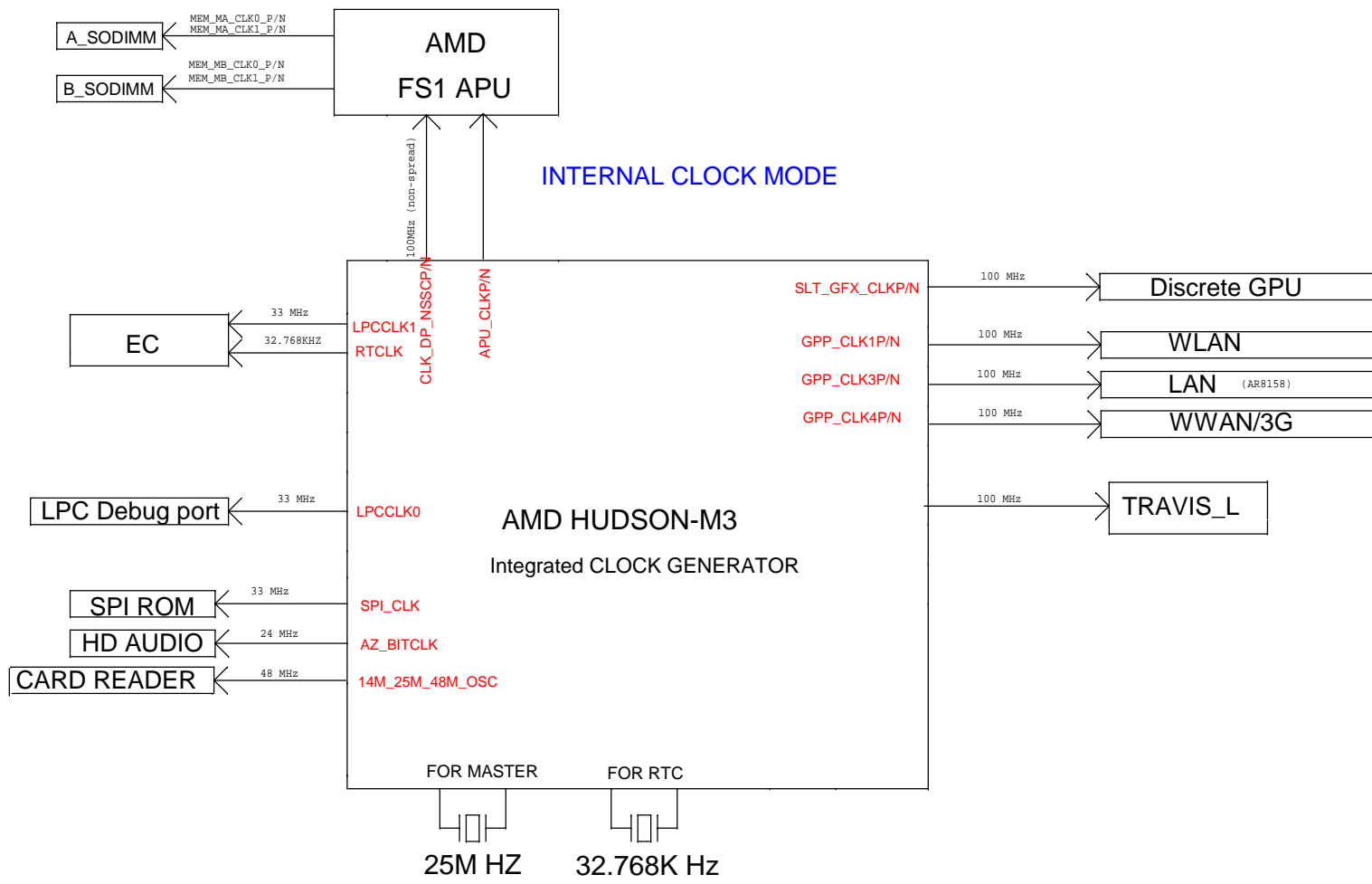
## TRAVIS\_L ANX3110 power on sequence

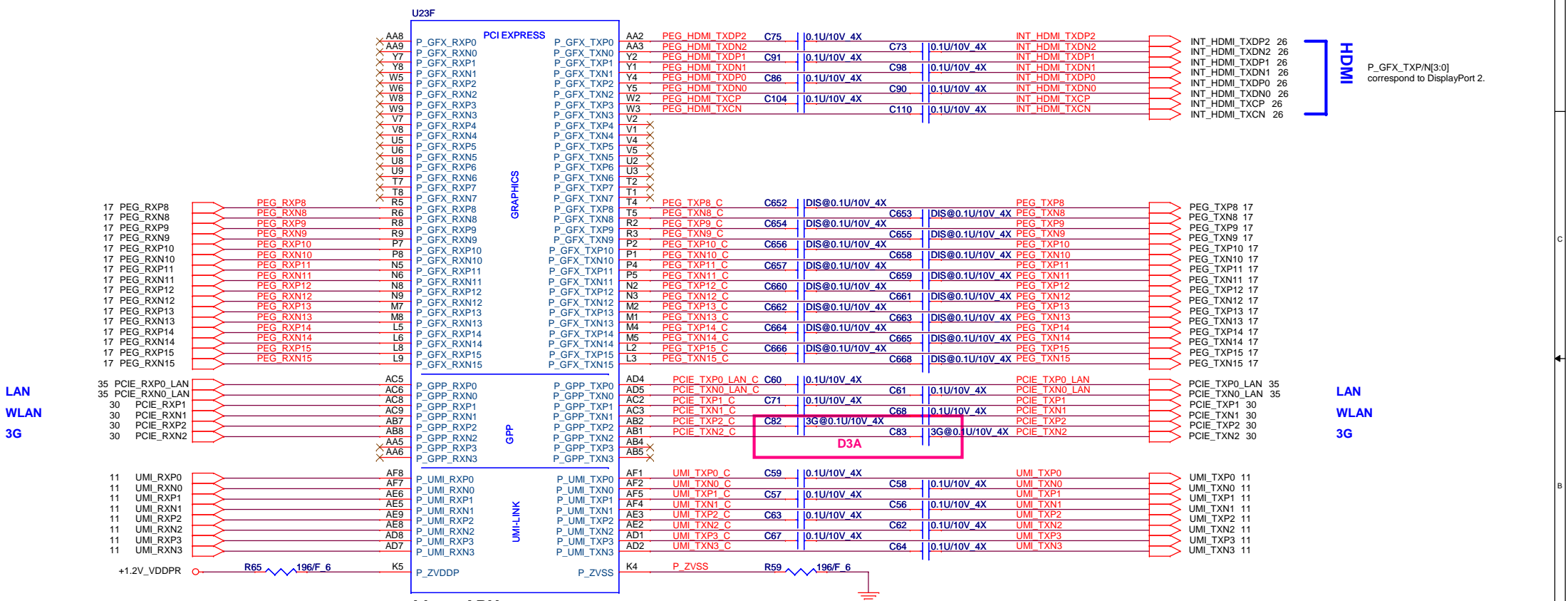
- 1.+3V must lead +1.2V\_TRAVIS

- 2.+1.2V\_TRAVIS must lead TRAVIS\_RST#

NOTE: FCH must output PCIE\_RST#\_TRAVIS or APU\_PCIE\_RST# after +1.2V\_TRAVIS ready



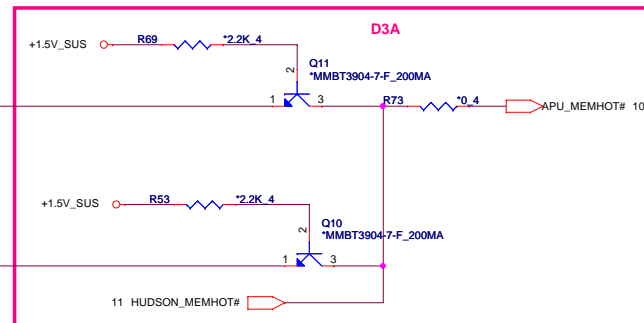
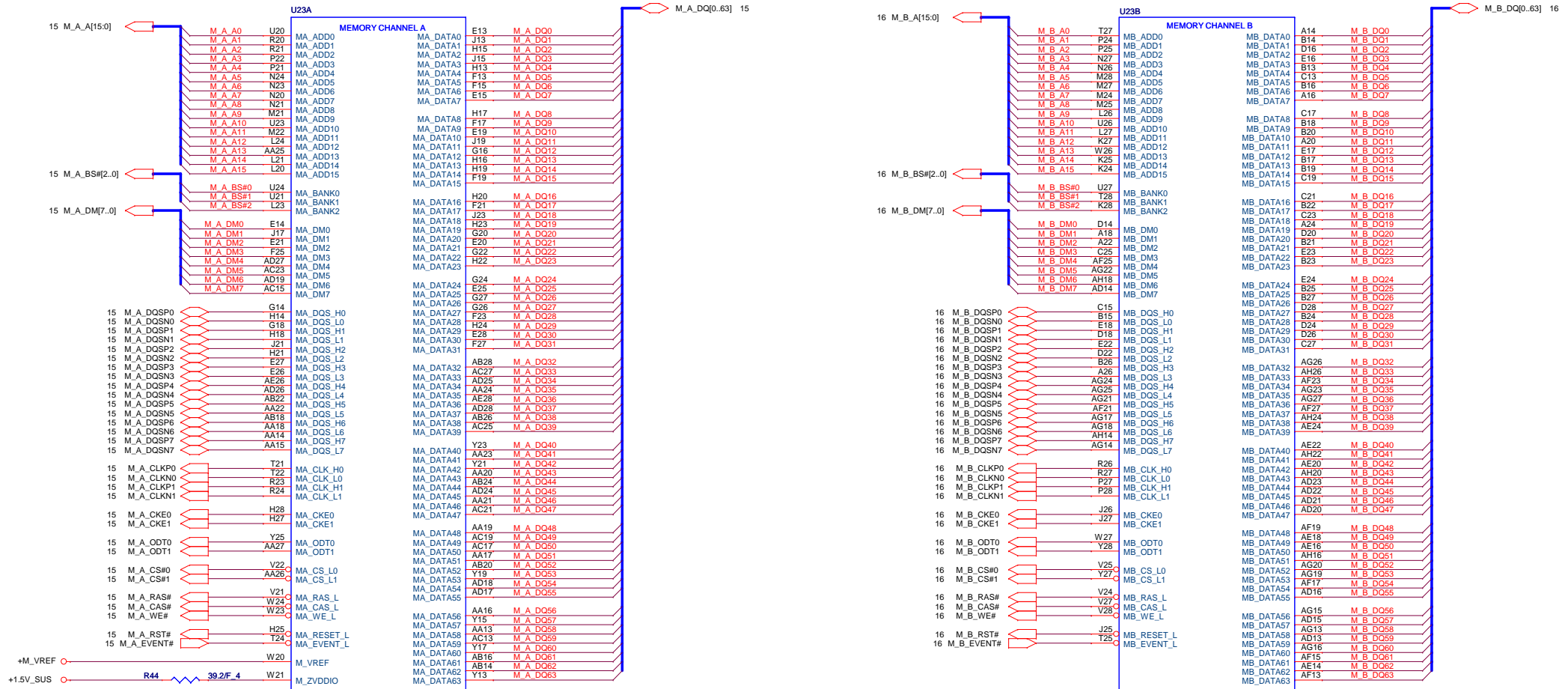




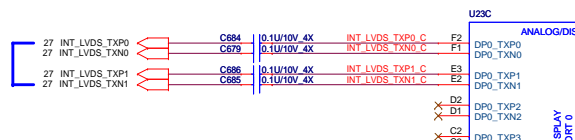
HDMI

P\_GFX\_TXP[N(3:0)] correspond to DisplayPort 2.

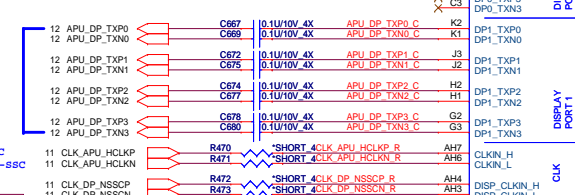
LAN  
WLAN  
3G



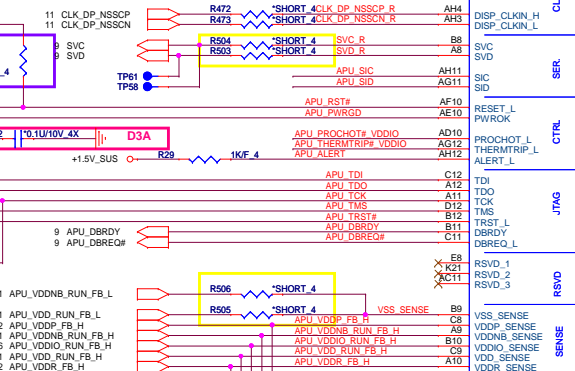
## DP0 to LVDS



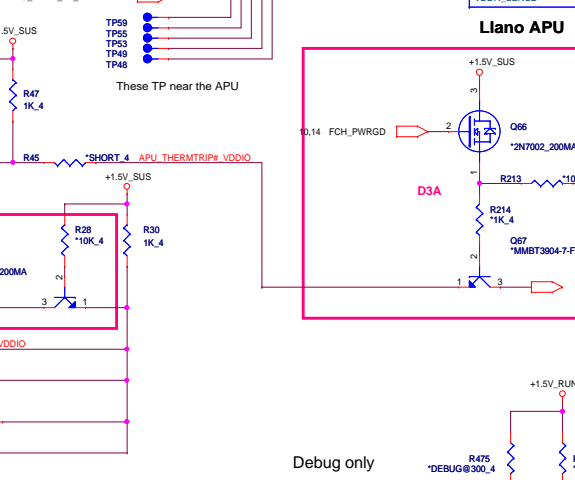
## DPI to Hudson-M3 VGA output



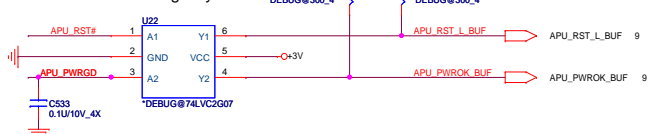
Note: CLK\_APU\_HCLKP/N is 100MHz SSC  
Note: CLK\_DP\_NSSCP/N is 100MHz non-SSC



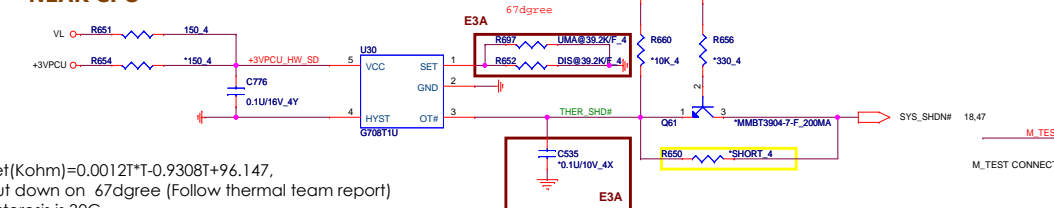
## L1ano APU



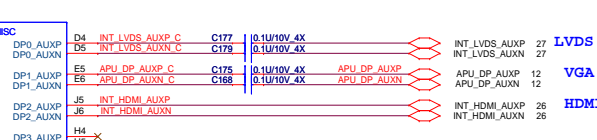
## Debug only



## NEAR CPU



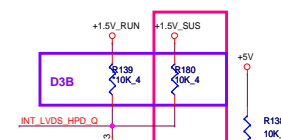
Rset(Kohm)=0.0012T-0.9308T+96.147,  
Shut down on 67degree (Follow thermal team report)  
Hysteresis is 30C



## LVDS

## VGA

## HDMI



## LVDS Hot-plug

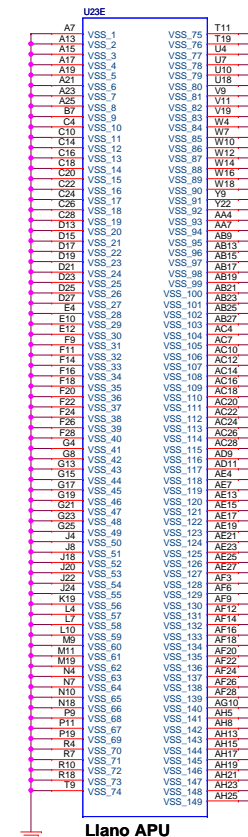
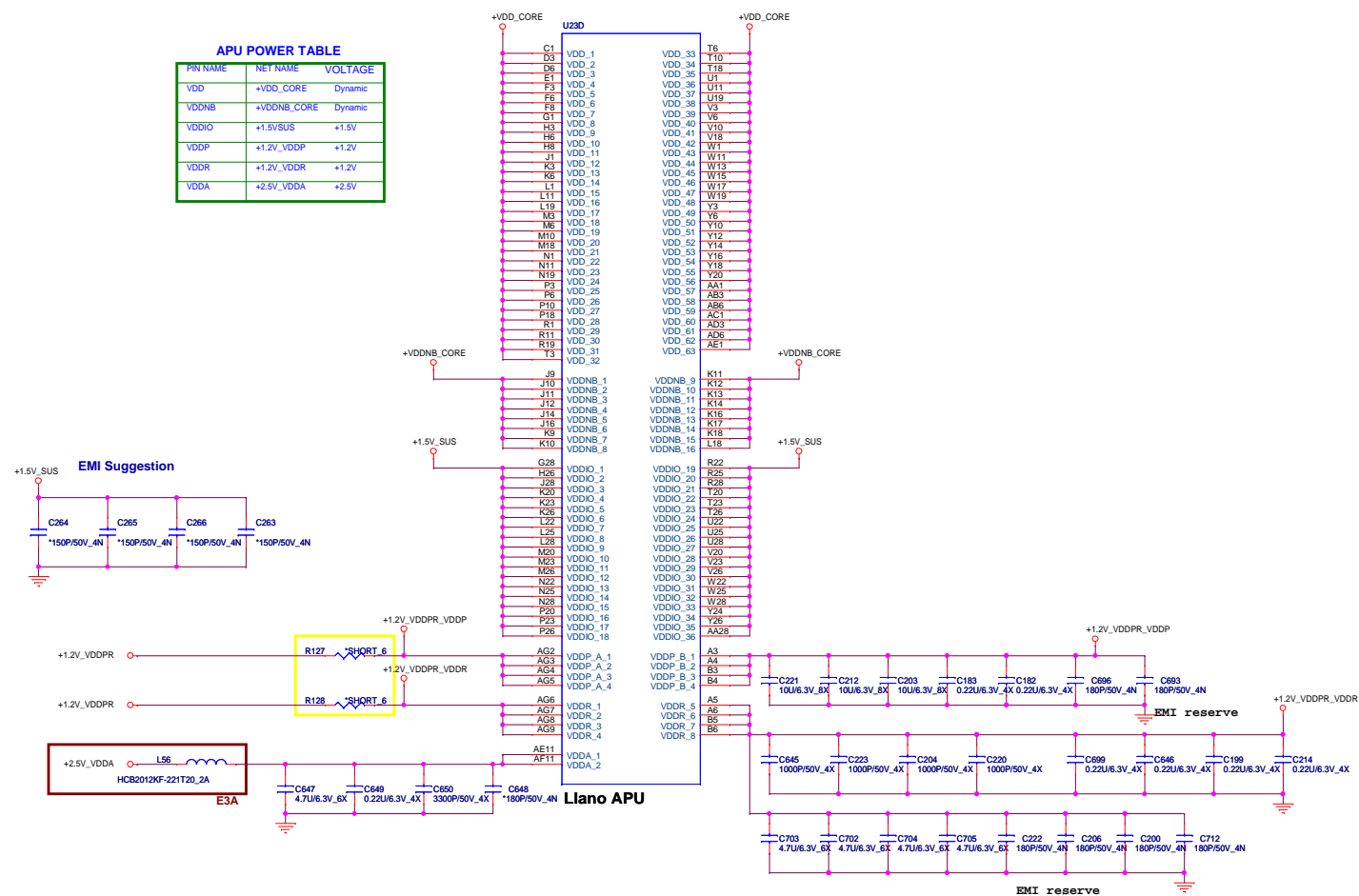


## CRT Hot-plug



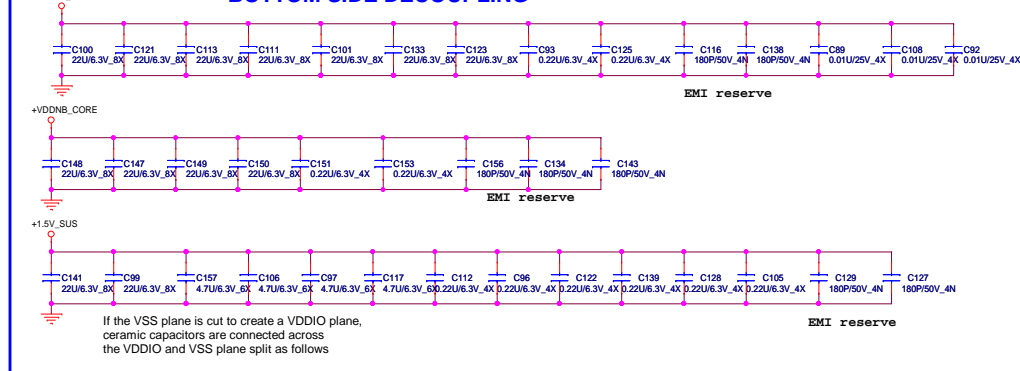
APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	Dynamic
VDDNB	+VDDNB_CORE	Dynamic
VDDIO	+1.5V_SUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



Liano APU

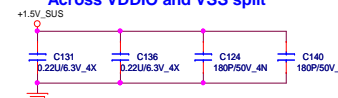
BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

DECOUPLING between PROCESSOR and DIMMs

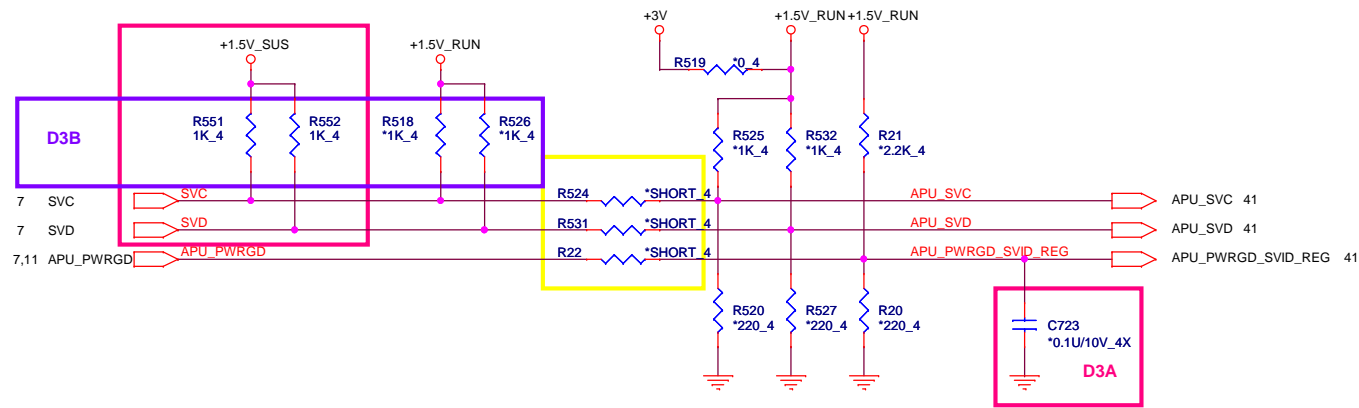
Across VDDIO and VSS split





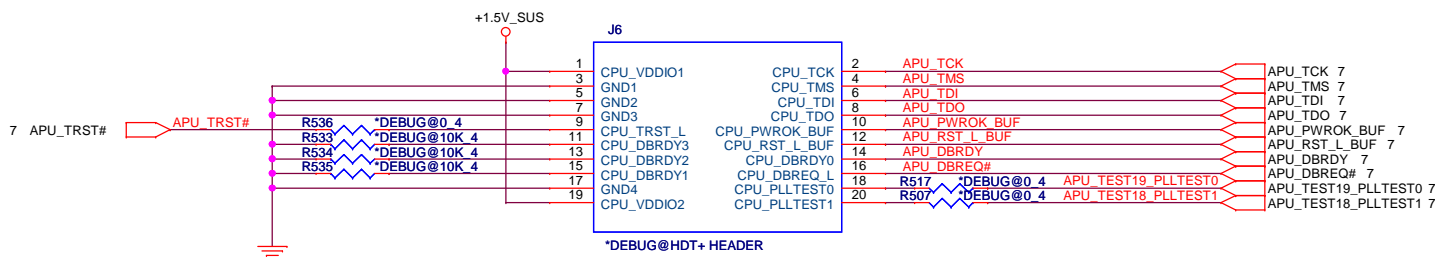
# VID Override Circuit

09



## HDT+ Connector

Debug only

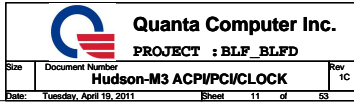


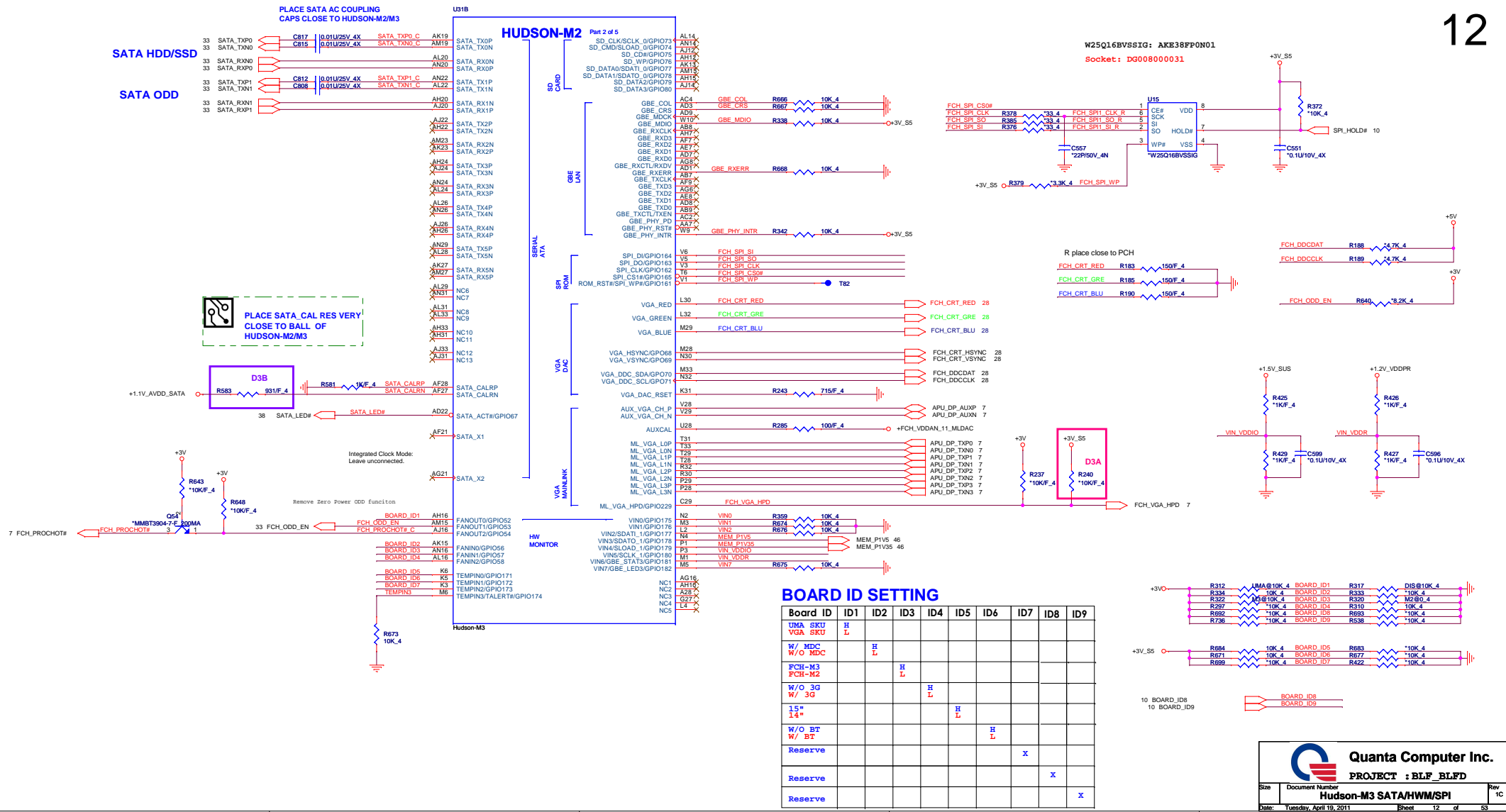
Quanta Computer Inc.

PROJECT : BLF\_BLF

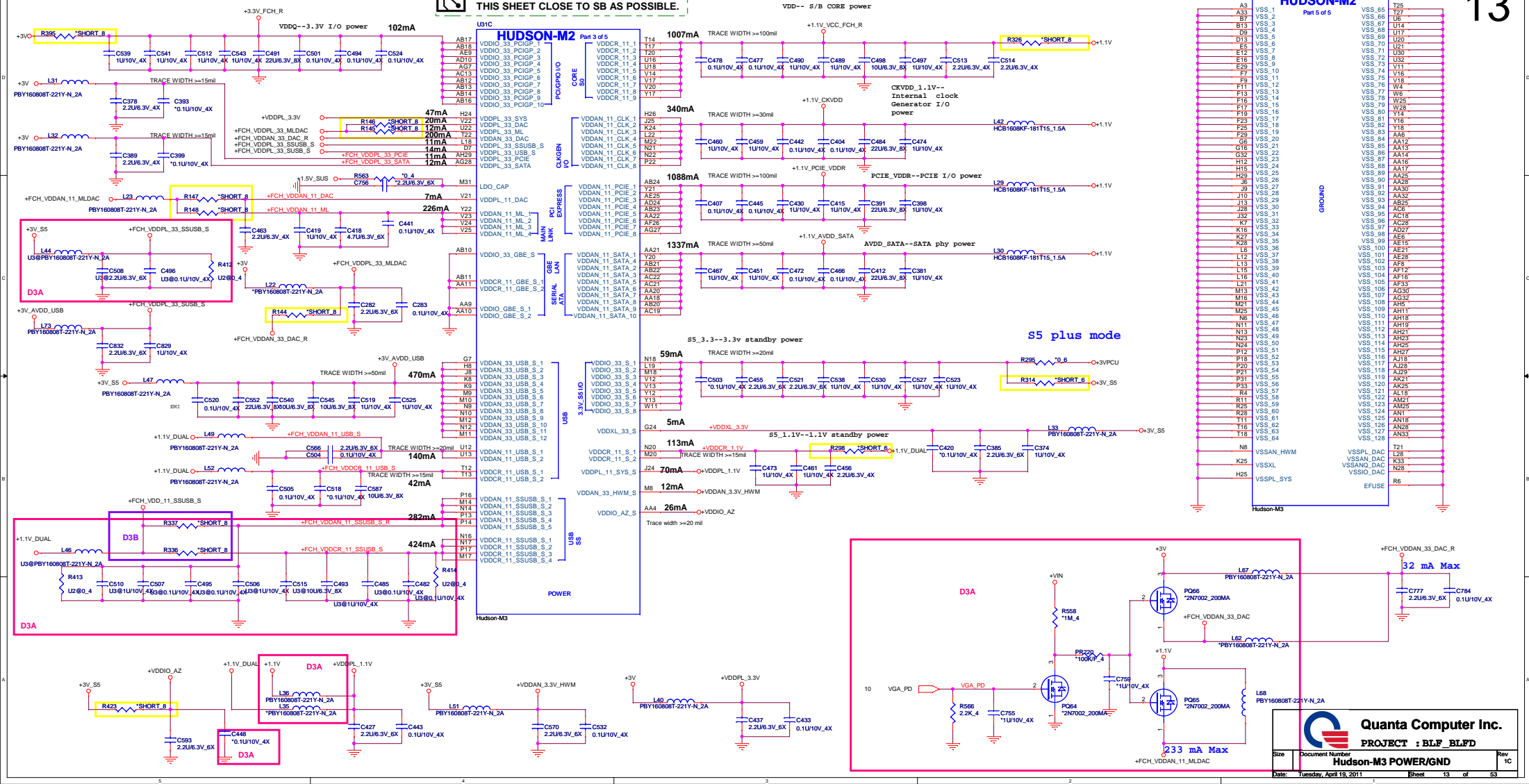
Size	Document Number	Rev
	Llano DEBUG&OTHER	1C
Date:	Tuesday, April 19, 2011	Sheet 9 of 53







PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



U3D

# HUDSON-M2

Part 5 of 5

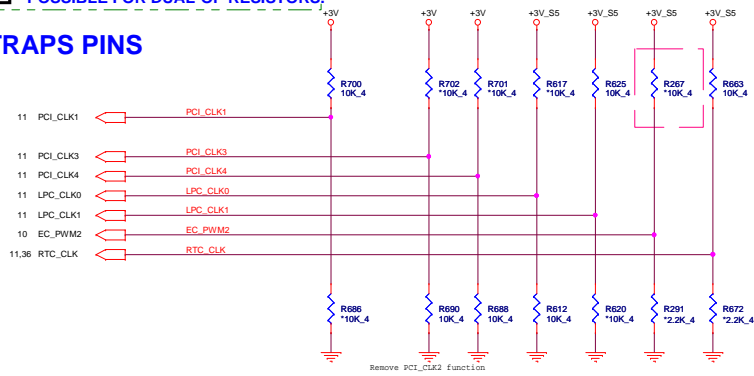
13

A3 VSS.1  
A31 VSS.2  
B7 VSS.3  
B13 VSS.4  
D9 VSS.5  
D13 VSS.6  
E7 VSS.7  
E12 VSS.8  
E16 VSS.9  
E20 VSS.10  
E24 VSS.11  
F7 VSS.12  
F11 VSS.13  
F15 VSS.14  
F19 VSS.15  
F23 VSS.16  
F27 VSS.17  
F31 VSS.18  
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F39 VSS.20  
F43 VSS.21  
F47 VSS.22  
F51 VSS.23  
F55 VSS.24  
F59 VSS.25  
F63 VSS.26  
F67 VSS.27  
F71 VSS.28  
F75 VSS.29  
F79 VSS.30  
F83 VSS.31  
F87 VSS.32  
F91 VSS.33  
F95 VSS.34  
F99 VSS.35  
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AW19 VSS.1080  
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AW67 VSS.1092  
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AW75 VSS.1094  
AW79 VSS.1095  
AW83 VSS.1096  
AW87 VSS.1097  
AW91 VSS.1098  
AW95 VSS.1099  
AW99 VSS.1100  
AX3 VSS.1101  
AX7 VSS.1102  
AX11 VSS.1103  
AX15 VSS.1104  
AX19 VSS.1105  
AX23 VSS.1106  
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AX31 VSS.1108  
AX35 VSS.1109  
AX39 VSS.1110  
AX43 VSS.1111  
AX47 VSS.1112  
AX51 VSS.1113  
AX55 VSS.1114  
AX59 VSS.1115  
AX63 VSS.1116  
AX67 VSS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

## STRAPS PINS



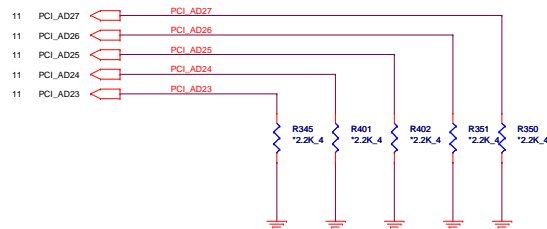
EC\_PWM2-->  
SPI ROM: 2.2-KΩ 5k pull-down  
LPC ROM: Pull-up to 3.3V\_S5.  
External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V\_S5.

## REQUIRED STRAPS

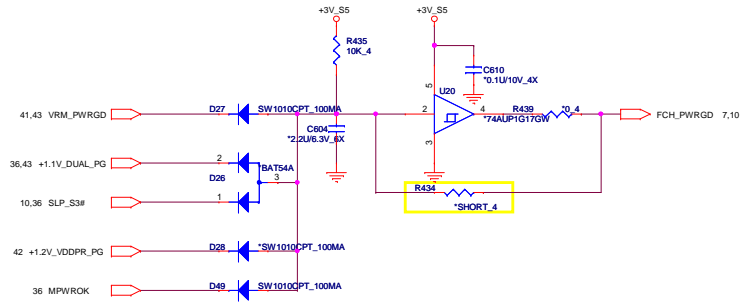
		PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	*****	ALLOW PCIe Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*****	FORCE PCIe Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



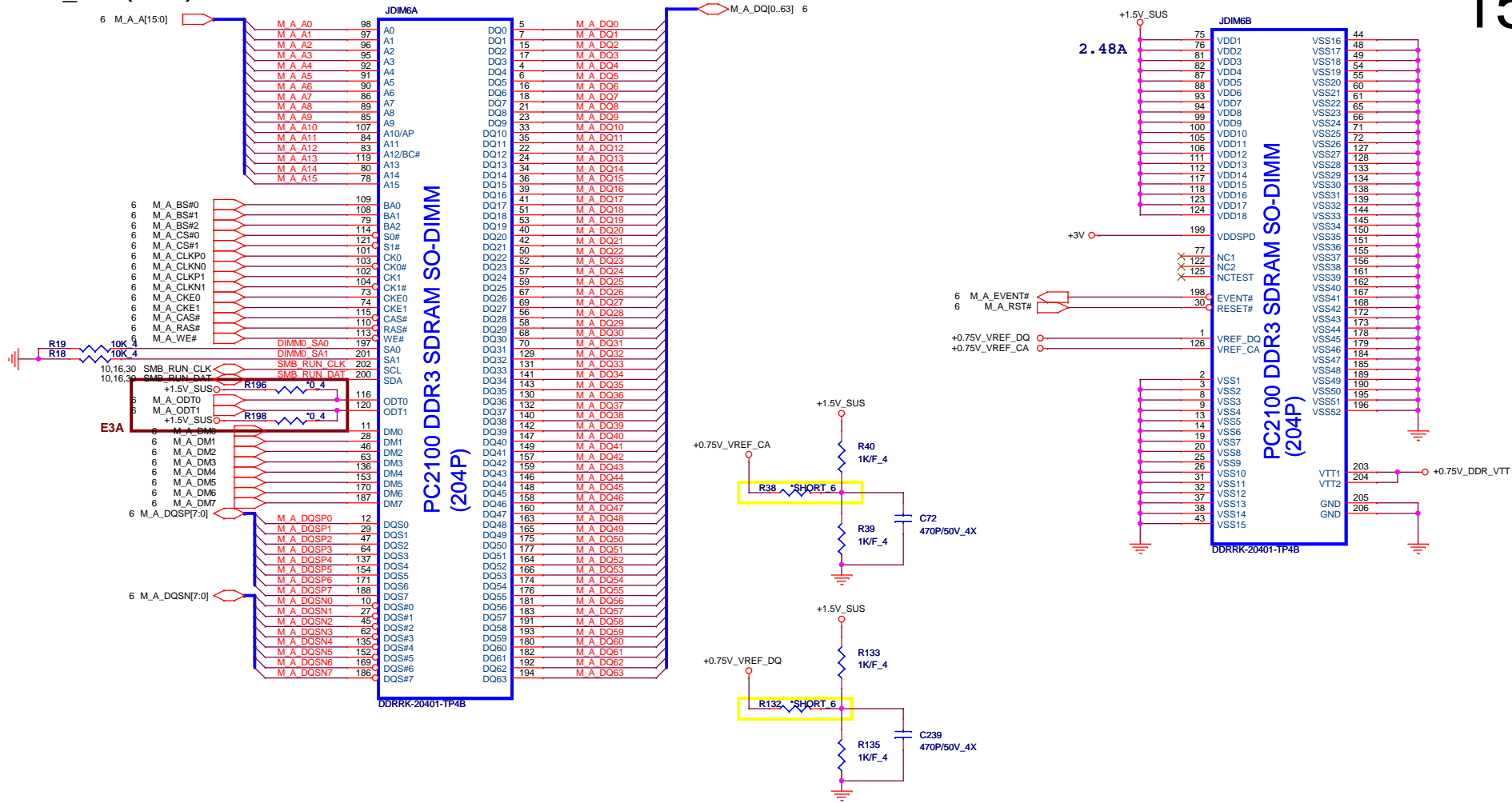
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT



FCH PWRGD CKT

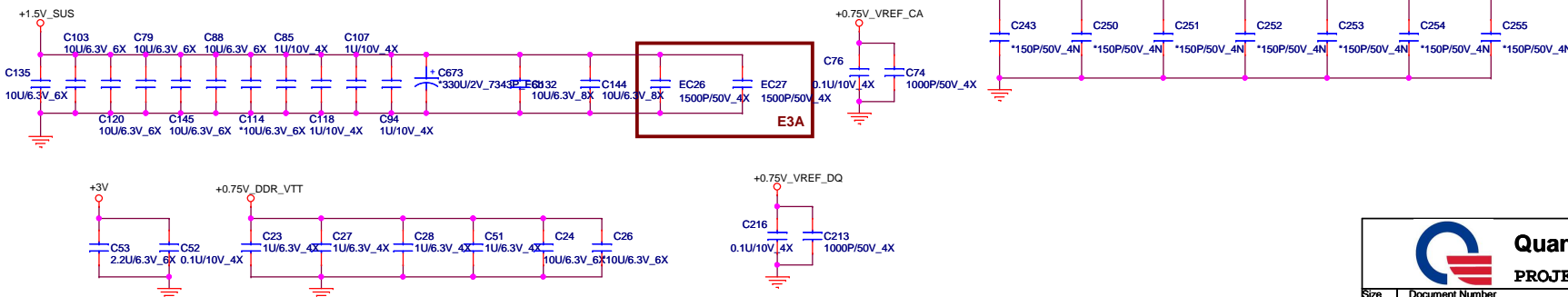
# DDR STD (DDR)

15

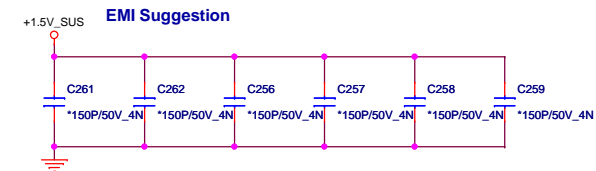
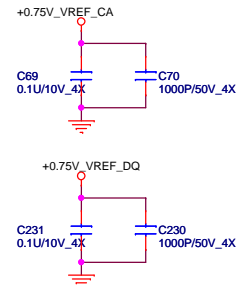
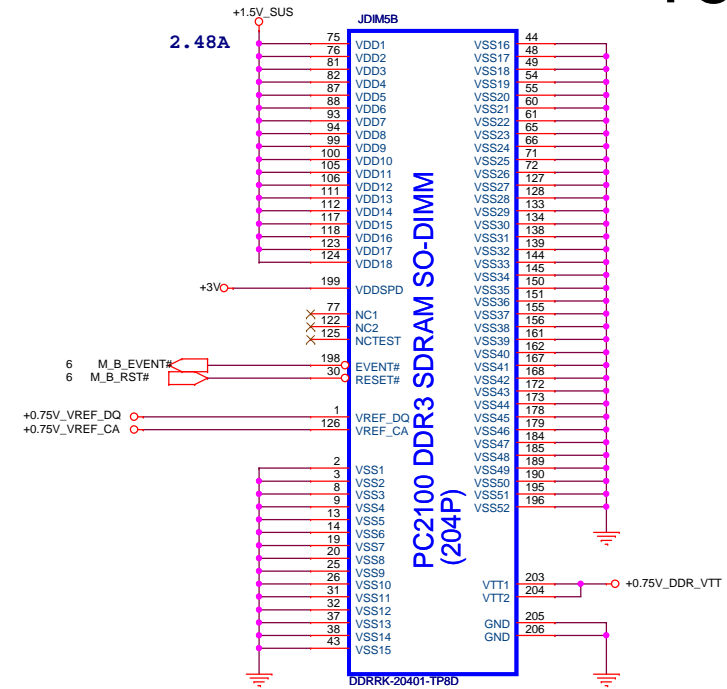


Place these Caps near SoDimm0.

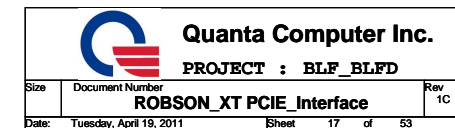
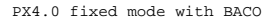
EMI Suggestion

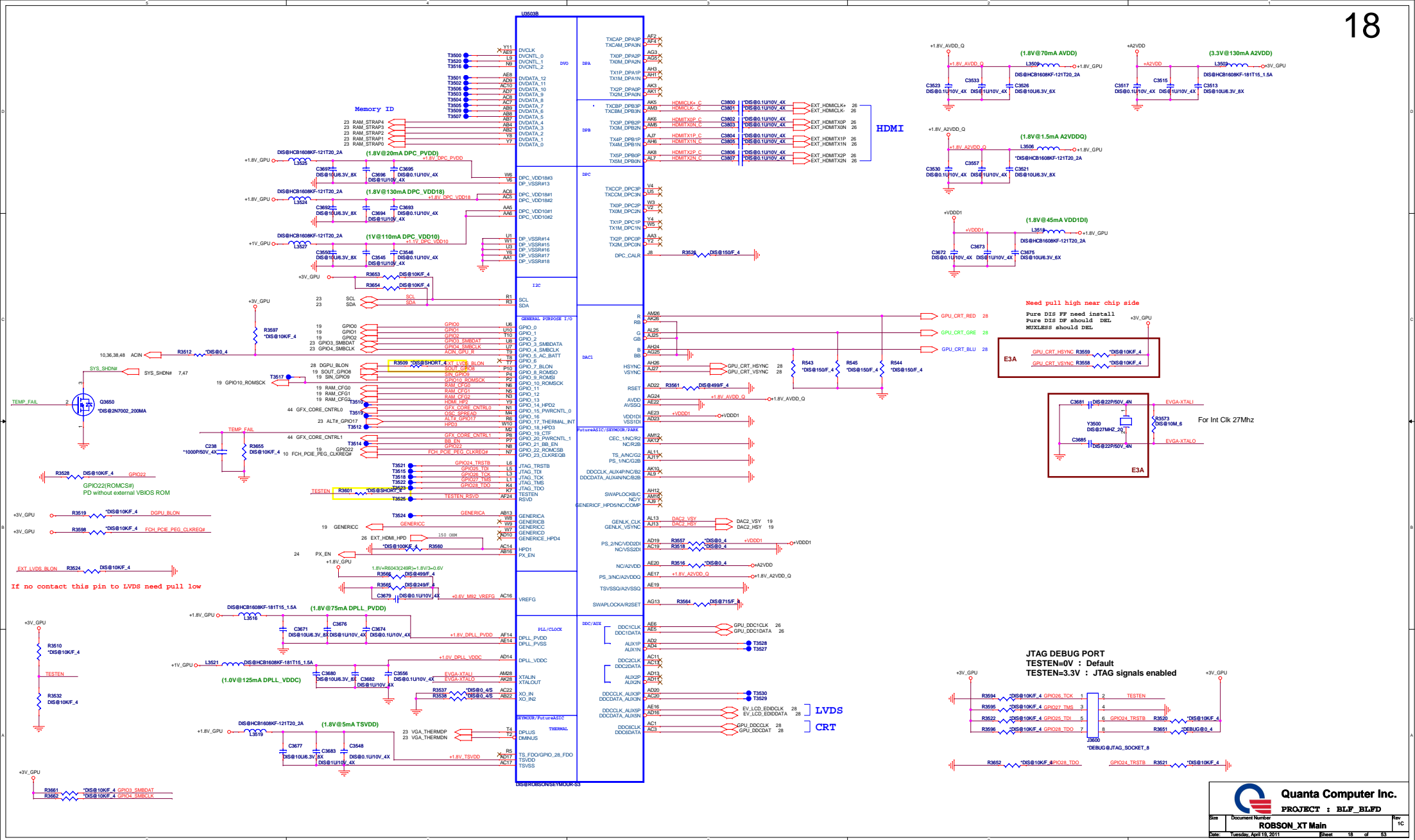


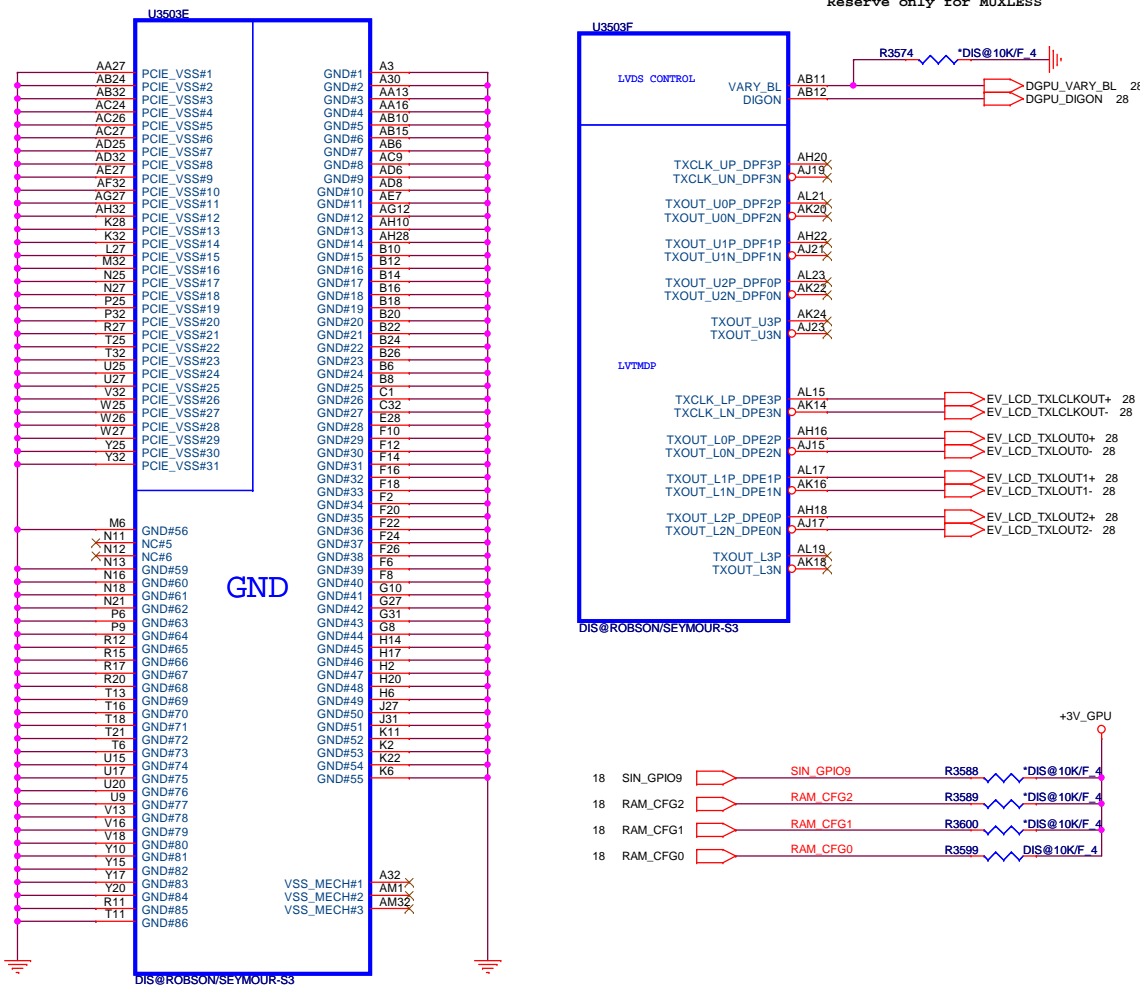


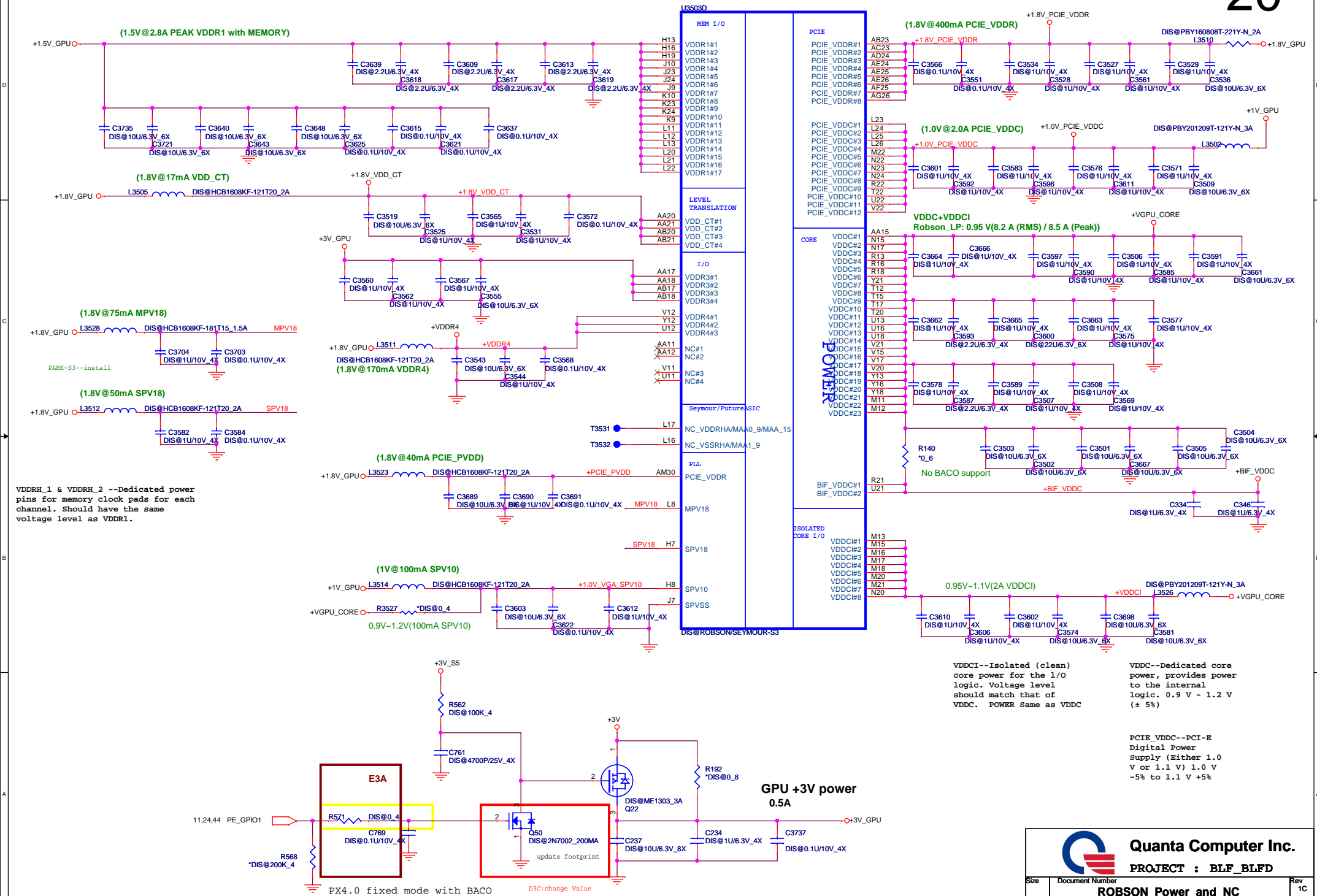


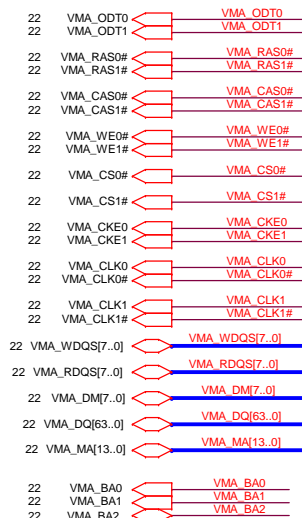






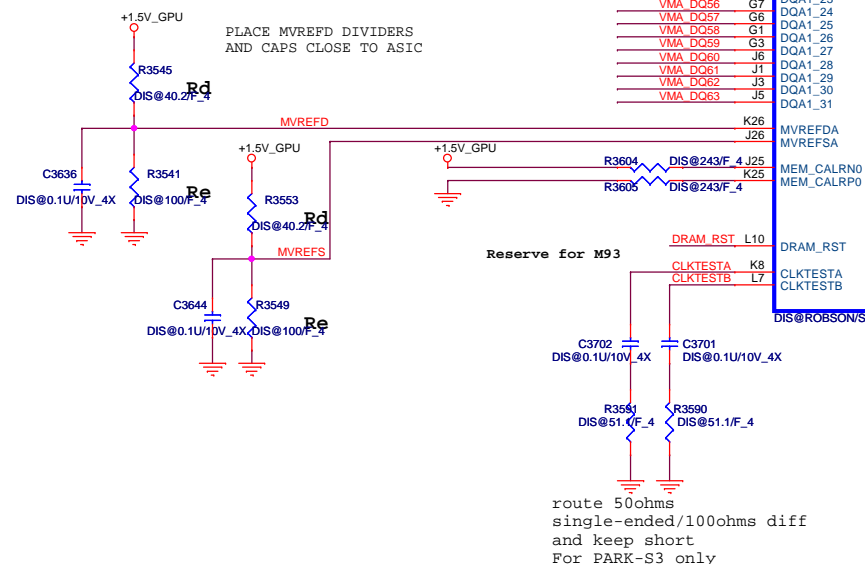






support 1gbt  
VRAM ( 64M X 16 )

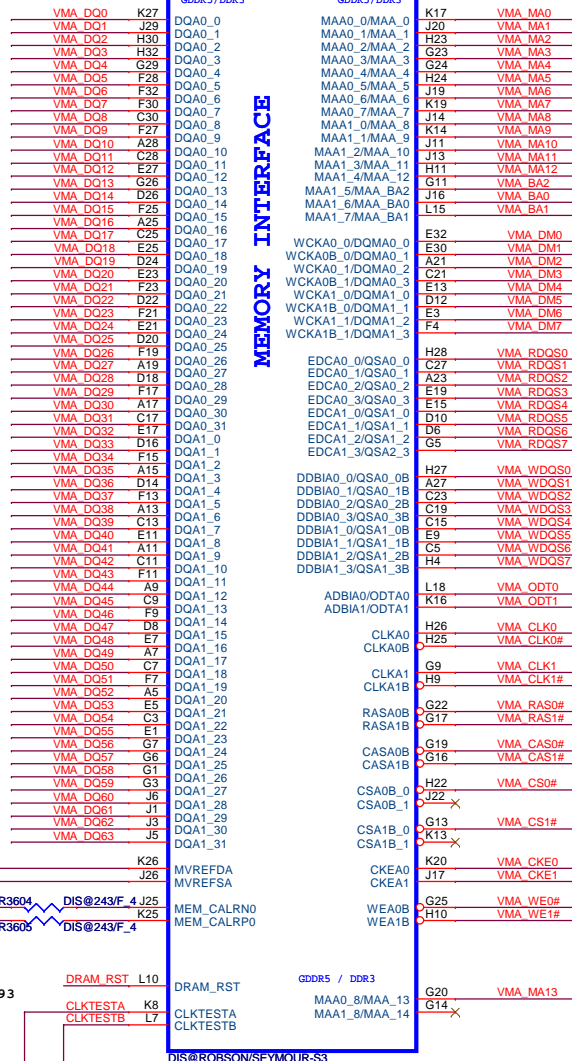
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



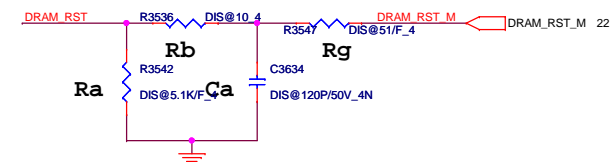
U3503C

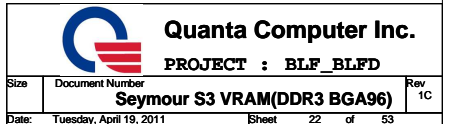
GDDR5 / DDR3

## MEMORY INTERFACE



Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R





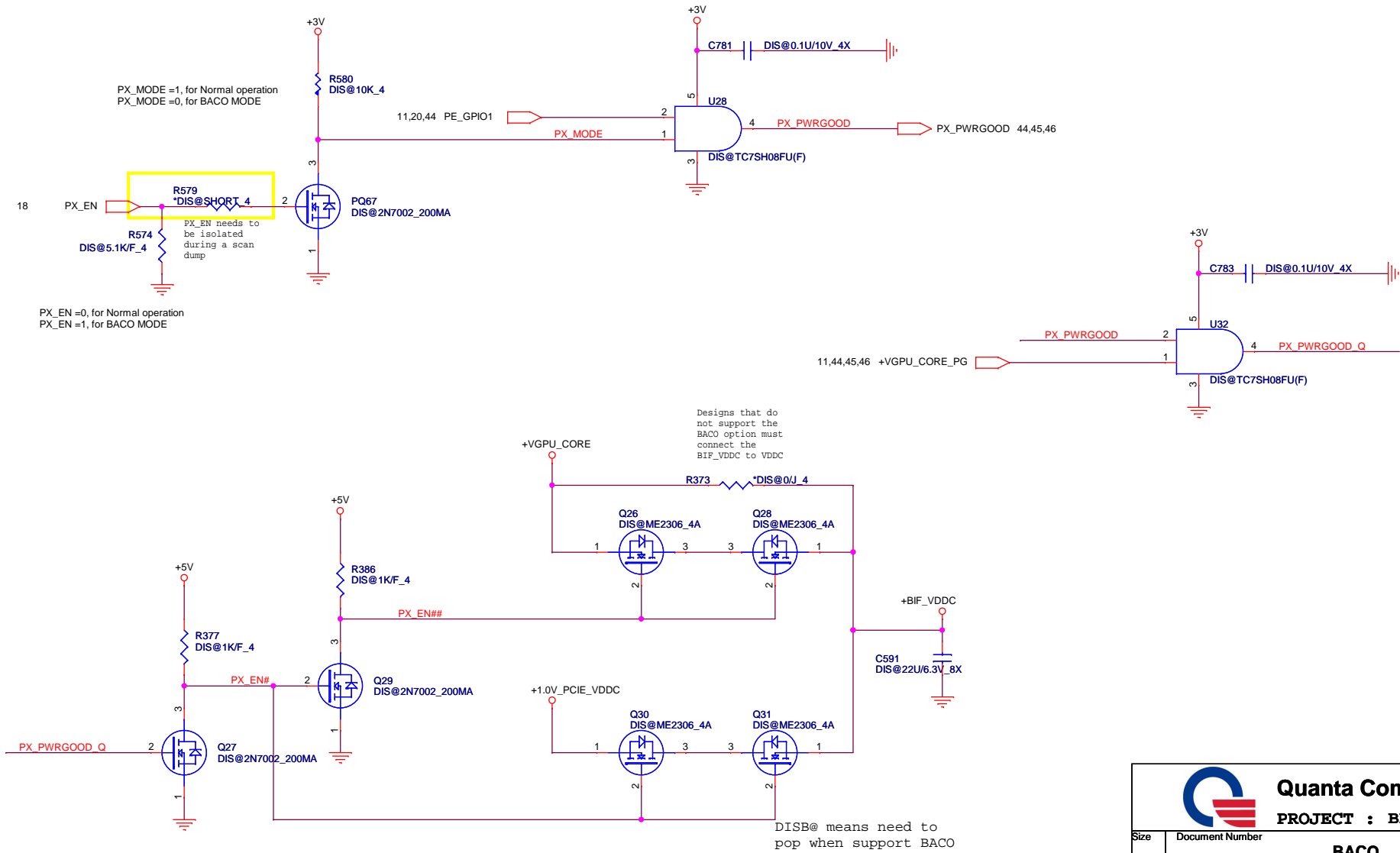


Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	1	0	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTT00 (128M*16-2Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	1	0	1	0	1
	K4W2G1646G-HC11	AKD5MGWTT500 (128M*16-2Gb)	1GB	0	0	0	1	0	1

# Sensor


The schematic diagram illustrates the Sensor module's internal components and its connections to the GPU, GPU04, and GPU03. The module includes a U25 sensor chip, several resistors (R547, R553, R549, R556), and capacitors (C739, C746). The connections are as follows:

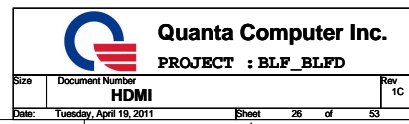
- GPU Connections:**
  - 36 3ND\_MBCLK:** Connected to the GPU's 36 3ND\_MBCLK pin.
  - 36 3ND\_MBDATA:** Connected to the GPU's 36 3ND\_MBDATA pin.
  - +3V\_GPU:** Connected to the GPU's +3V\_GPU pin.
- GPU04 Connections:**
  - 18 SCL:** Connected to the GPU04's SCL pin.
  - 18 SDA:** Connected to the GPU04's SDA pin.
  - 18 GPIO04\_SMBCLK:** Connected to the GPU04's GPIO04\_SMBCLK pin.
  - 18 GPIO03\_SMBCLK:** Connected to the GPU03's SMBCLK pin.
- GPU03 Connections:**
  - 18 ALT#\_GPIO17:** Connected to the GPU03's ALT#\_GPIO17 pin.
  - 39 VGA\_THERM#:** Connected to the GPU03's VGA\_THERM# pin.
- Internal Components:**
  - U25:** Sensor chip with ADDRESS 96H.
  - R547, R553, R549, R556:** Resistors with values 4.7K\_4, 4.7K\_4, 10K\_4, and 10K\_4 respectively.
  - C739, C746:** Capacitors with values 0.1u/10V\_4K and 2200p/50V\_4X respectively.

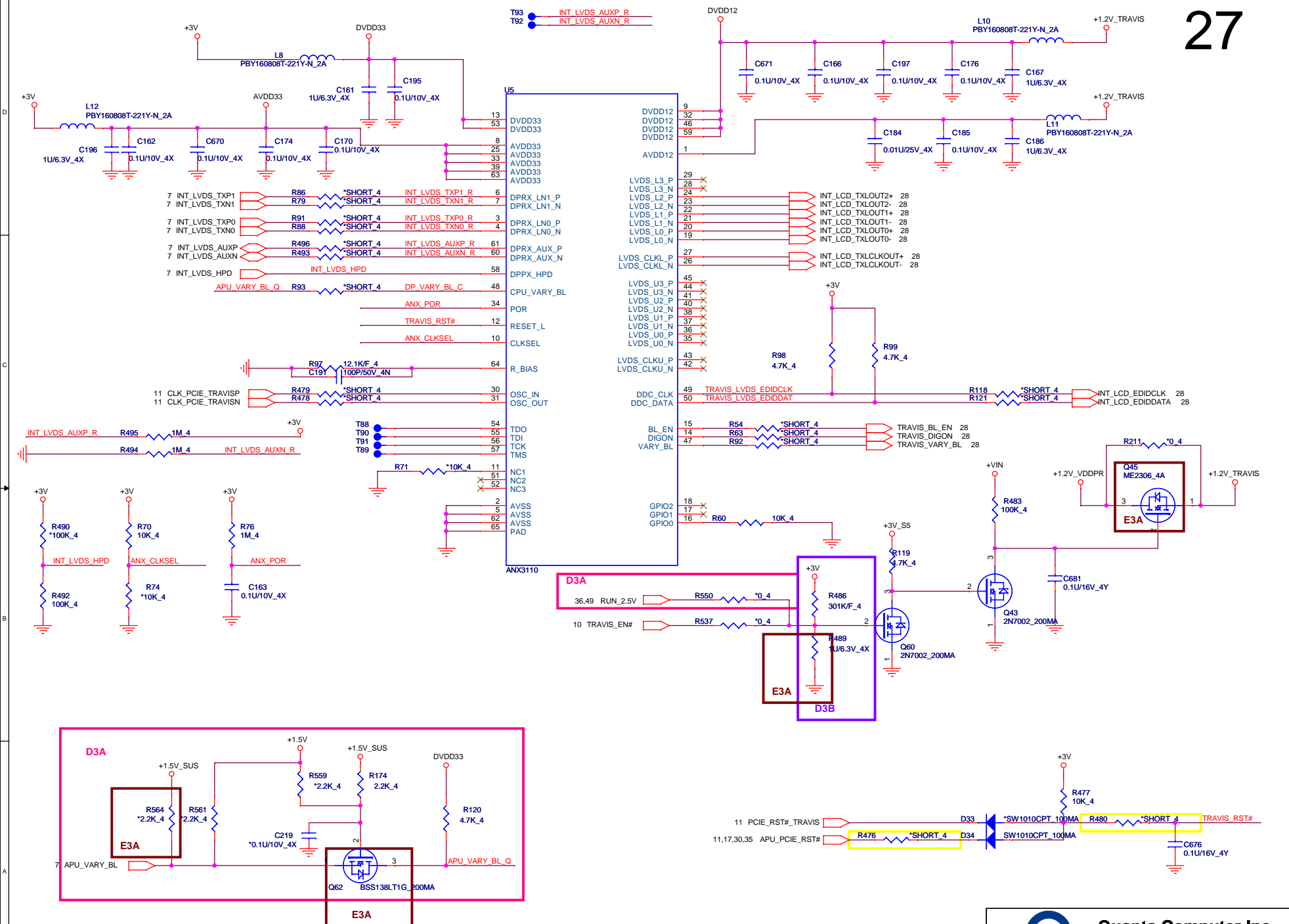


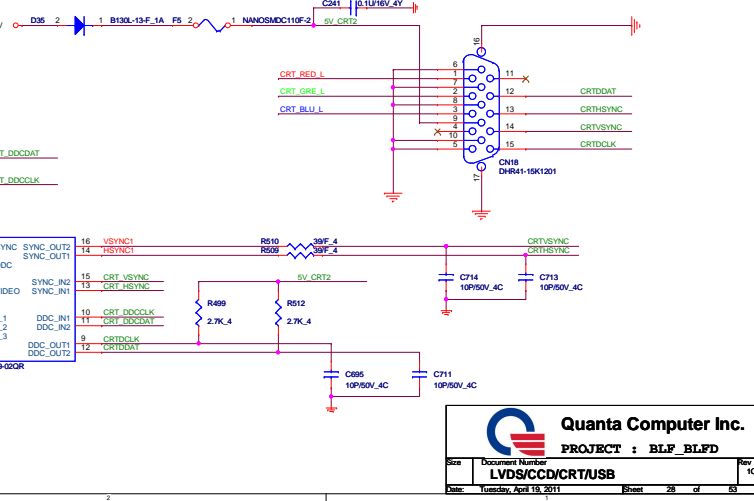
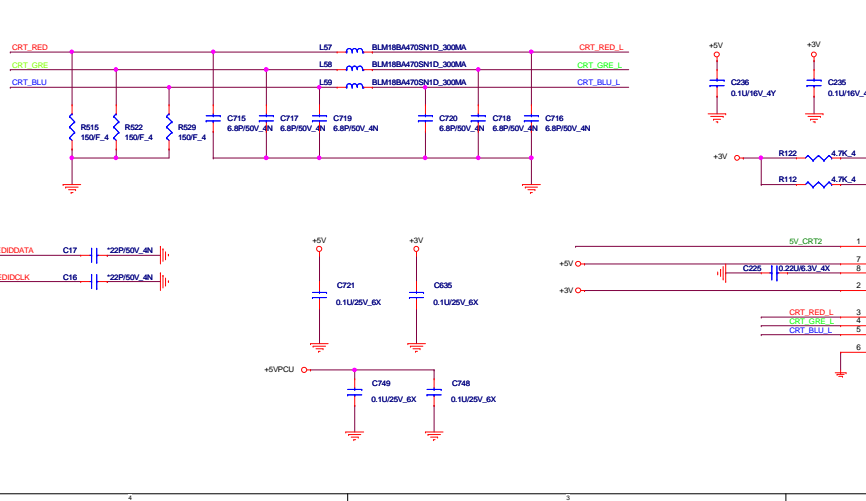
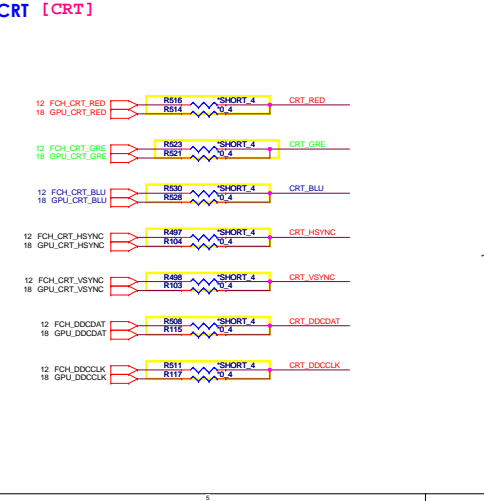
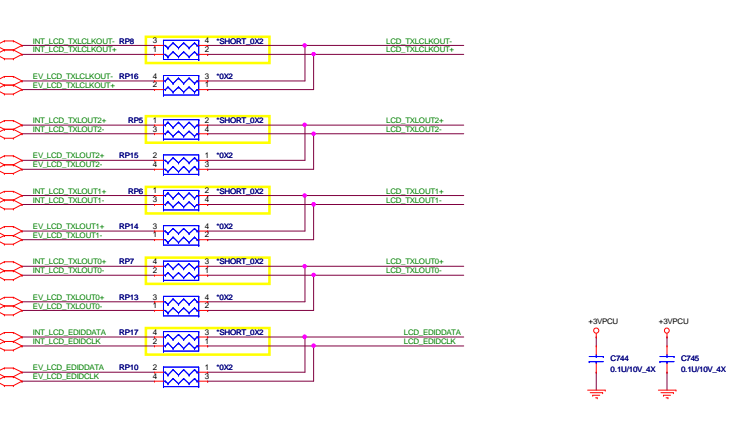
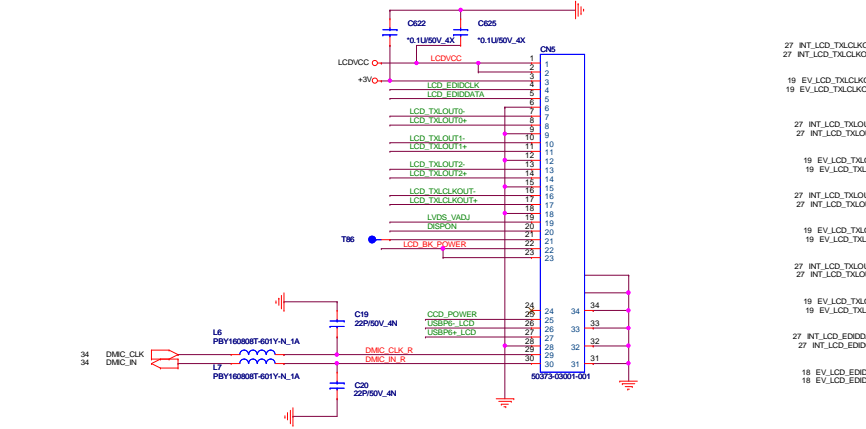
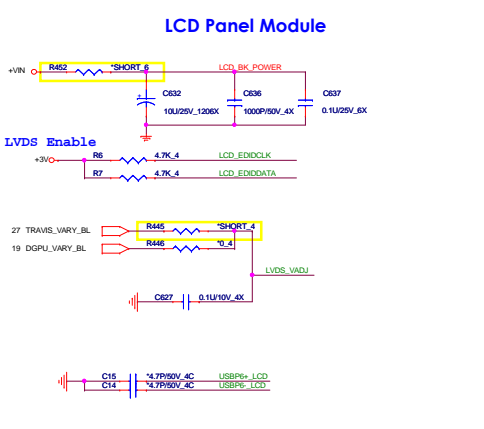
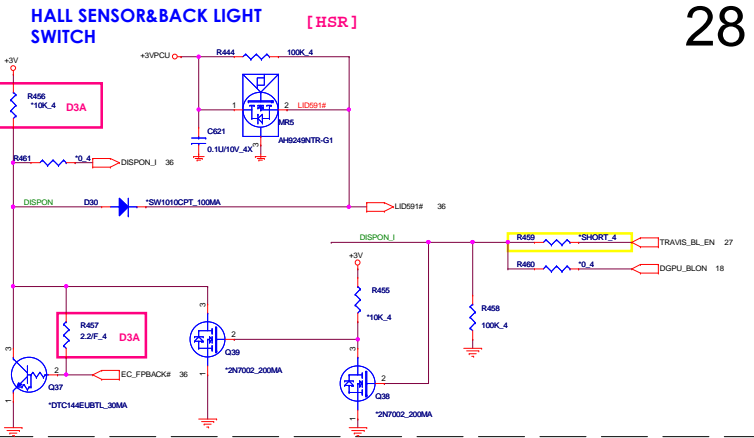
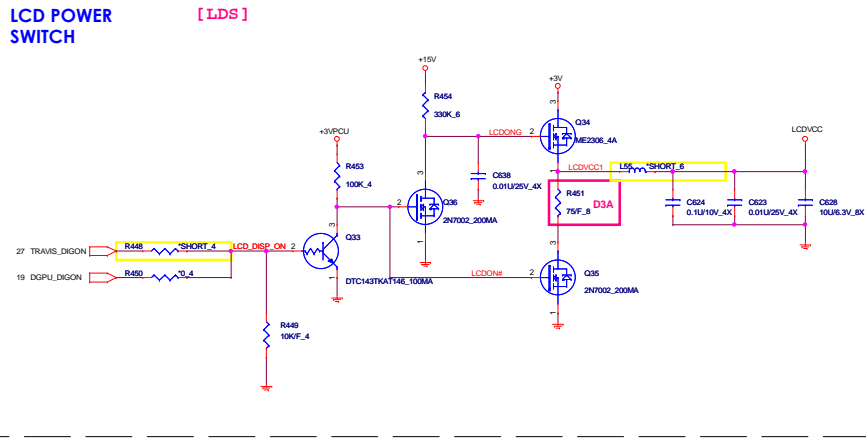
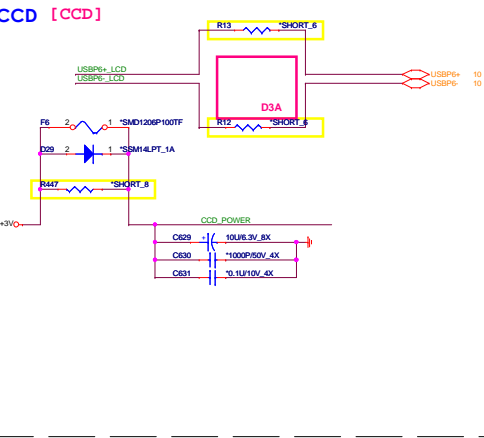


D										D
C										C
B										B
A										A

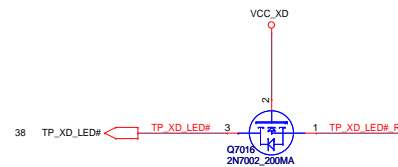
		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : BLF_BLFD</b>	
Size	Document Number		Rev
	<b>Blank</b>		<b>1C</b>
Date:	Tuesday, April 19, 2011		Sheet 25 of 53



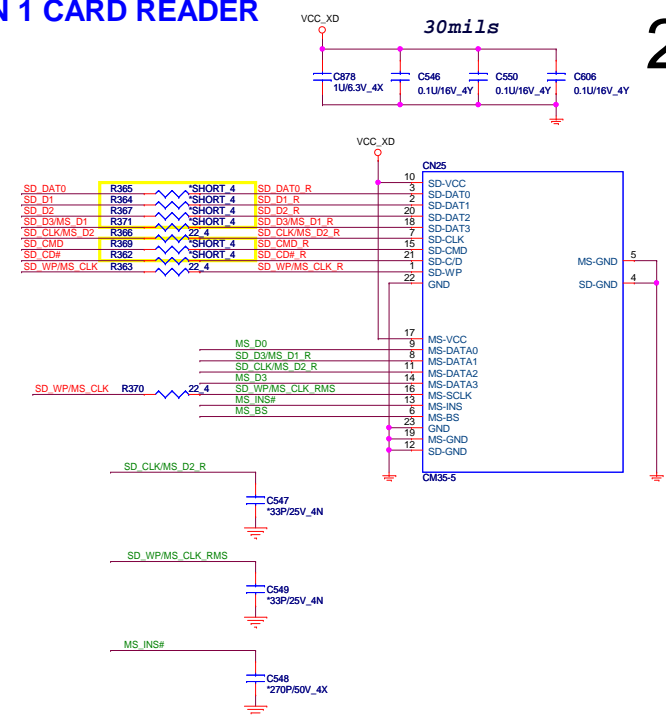




Card reader controller <MMC>



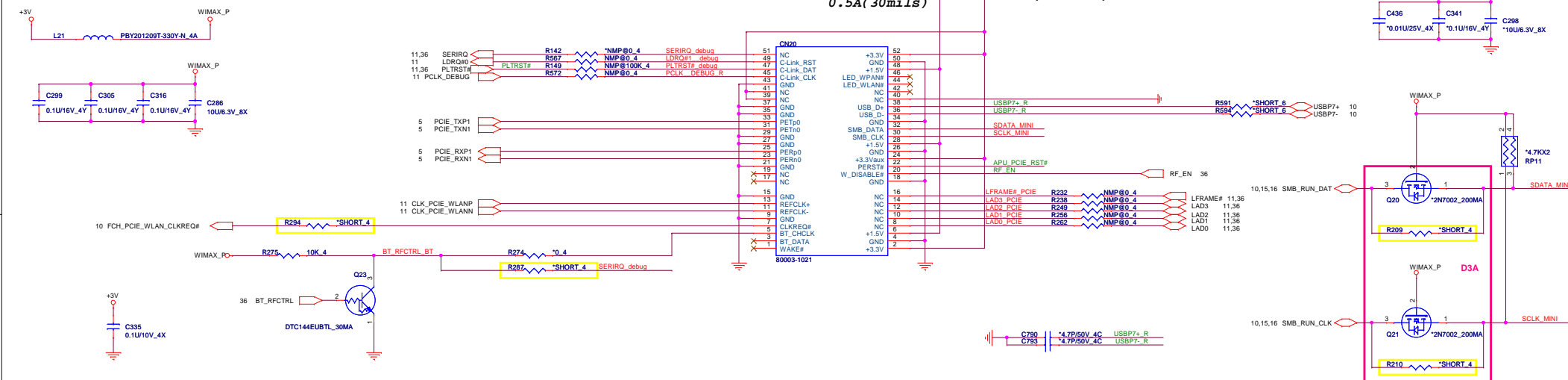
## 29

**Quanta Computer Inc.**

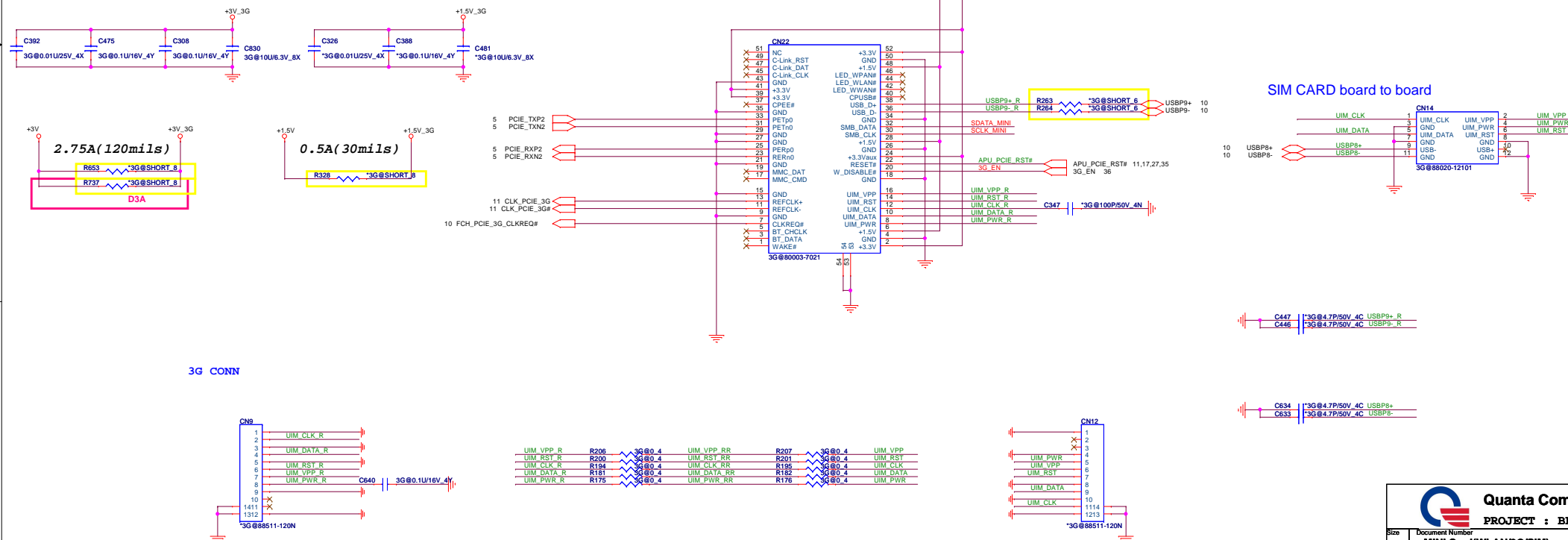
PROJECT : BLF\_BLFD

Size	Document Number	Rev
	<b>RTS5138 (Card Reader)</b>	1C
Date:	Tuesday, April 19, 2011	Sheet 29 of 53

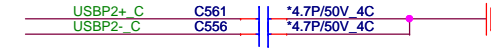
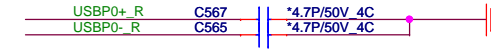
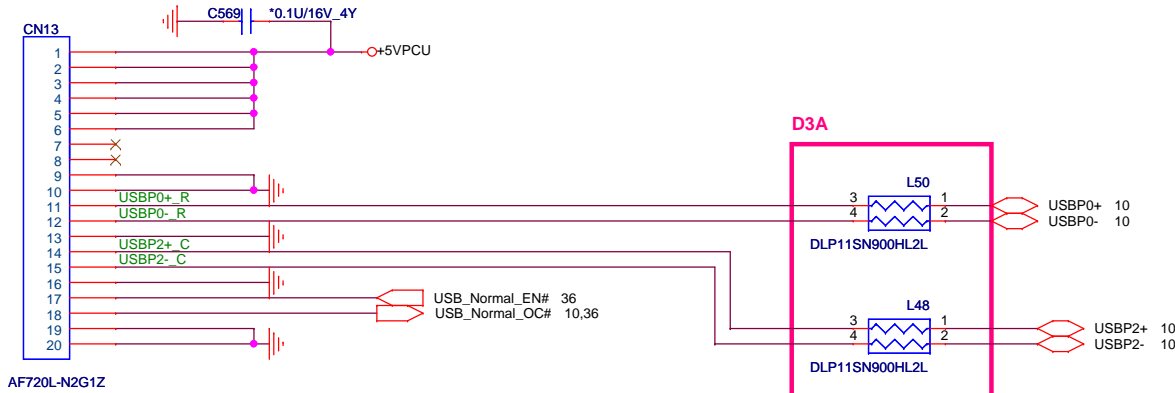
MINI Card Slot#1  
(WiFi)



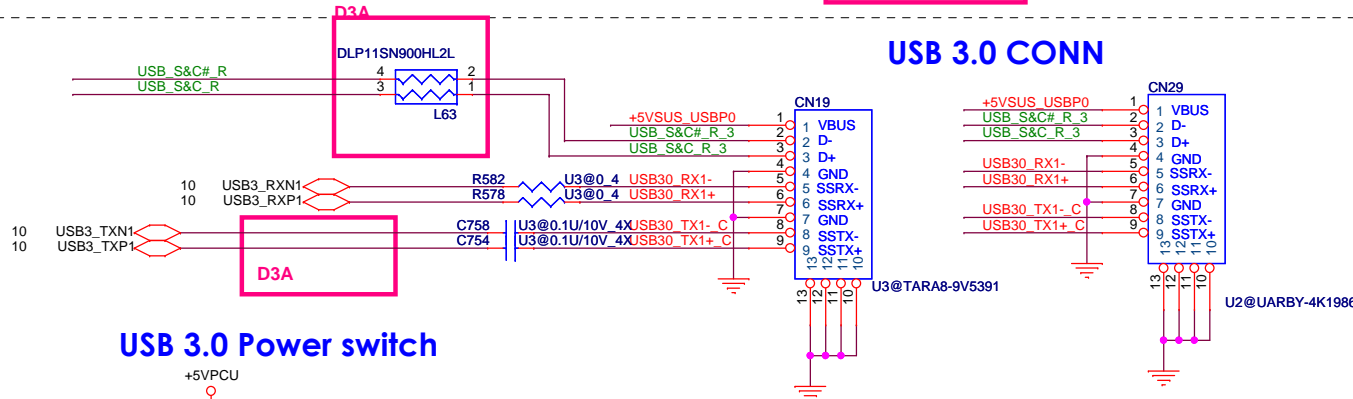
MINI Card Slot#2  
3G



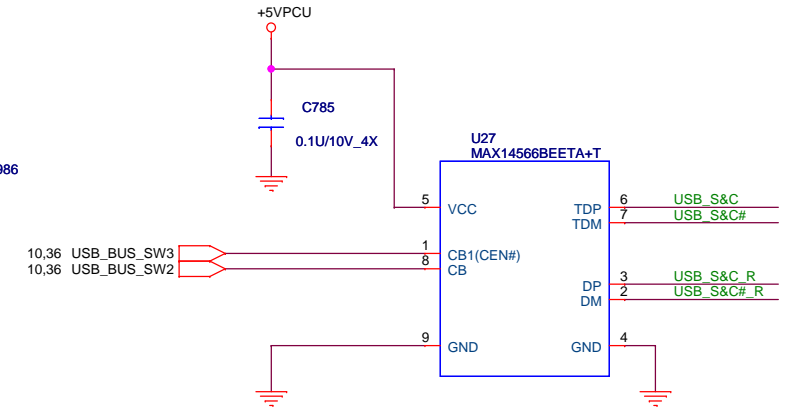
## USB board



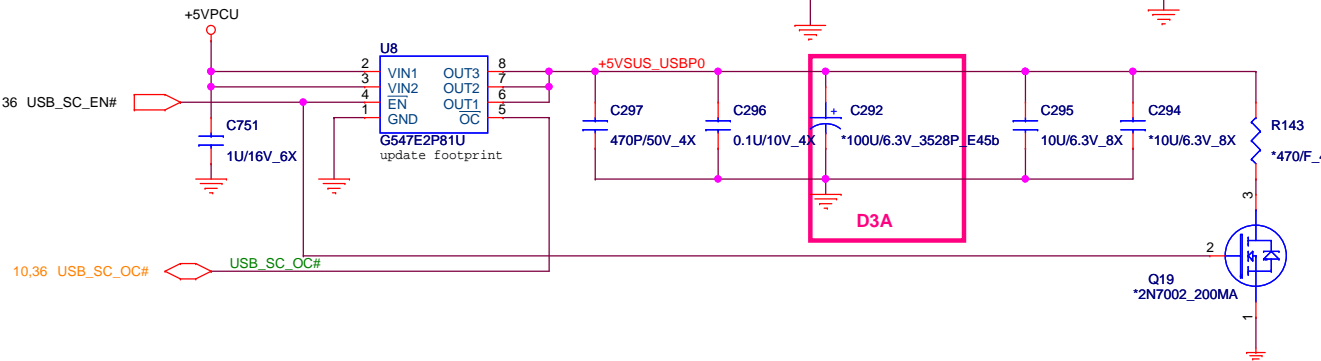
## USB 3.0 CONN



## USB Sleep & Charge MAXIM solution



## USB 3.0 Power switch



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM



Quanta Computer Inc.

PROJECT : BLF\_BLF

Size Document Number USB2.0X1+USB3.0X1 Rev 1C

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D

D

C

C

B

B

A

A



**Quanta Computer Inc.**

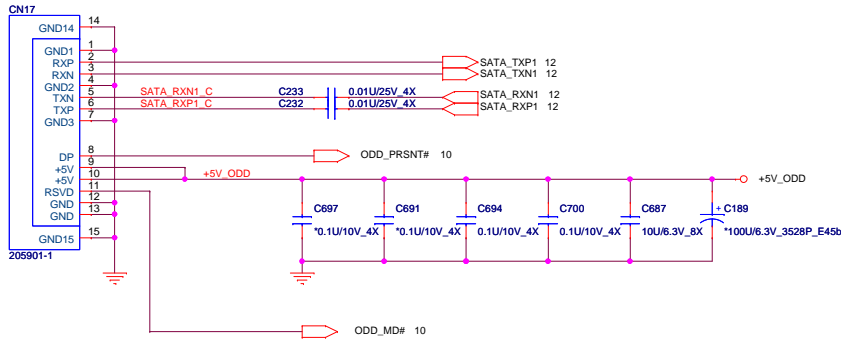
**PROJECT : BLF\_BLFD**

Size	Document Number	Rev
	<b>BLANK</b>	<b>1C</b>
Date:	Tuesday, April 19, 2011	Sheet 32 of 53

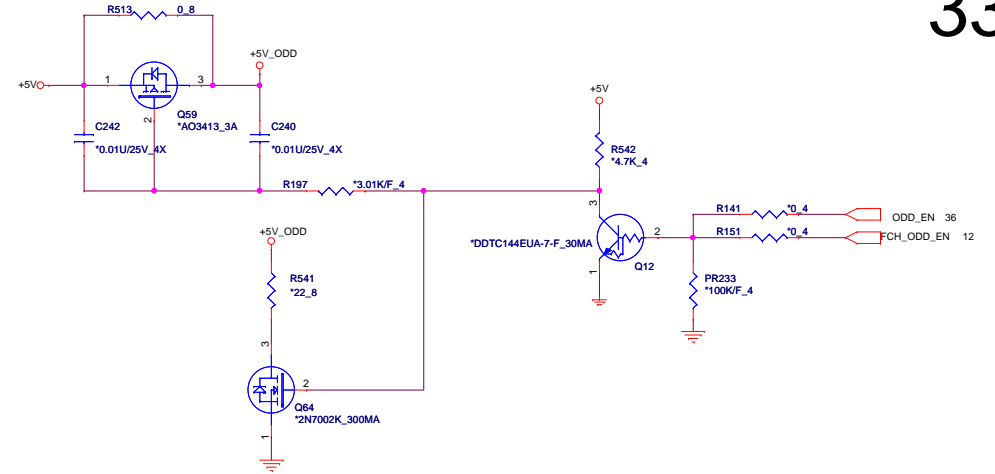


## SATA ODD

[ ODD ]

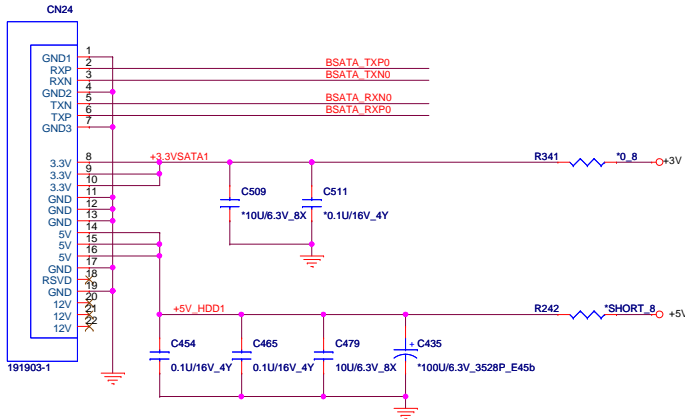


## ODD Zero power .

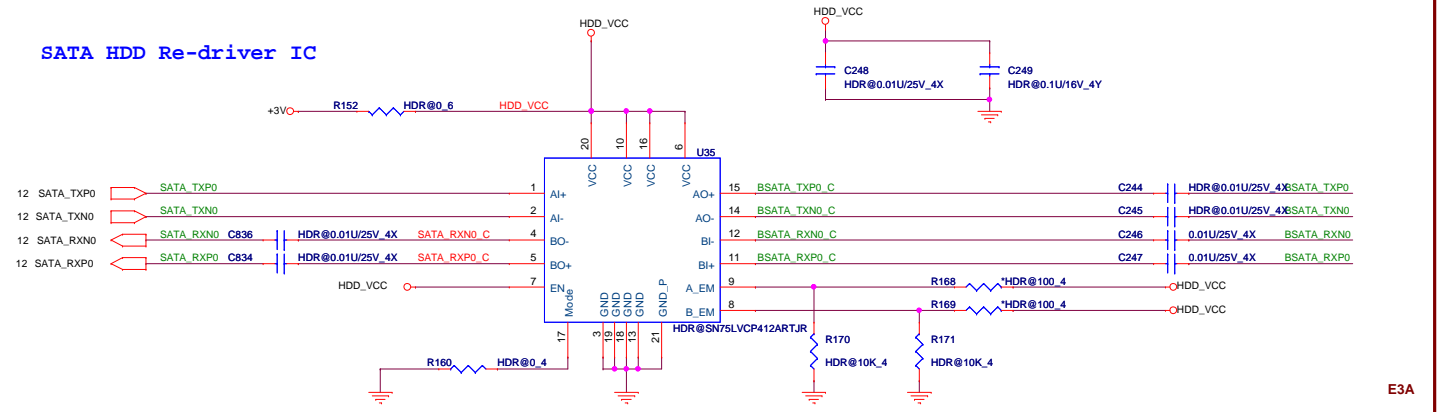


## SATA HDD

[ HDD ]



### SATA HDD Re-driver IC

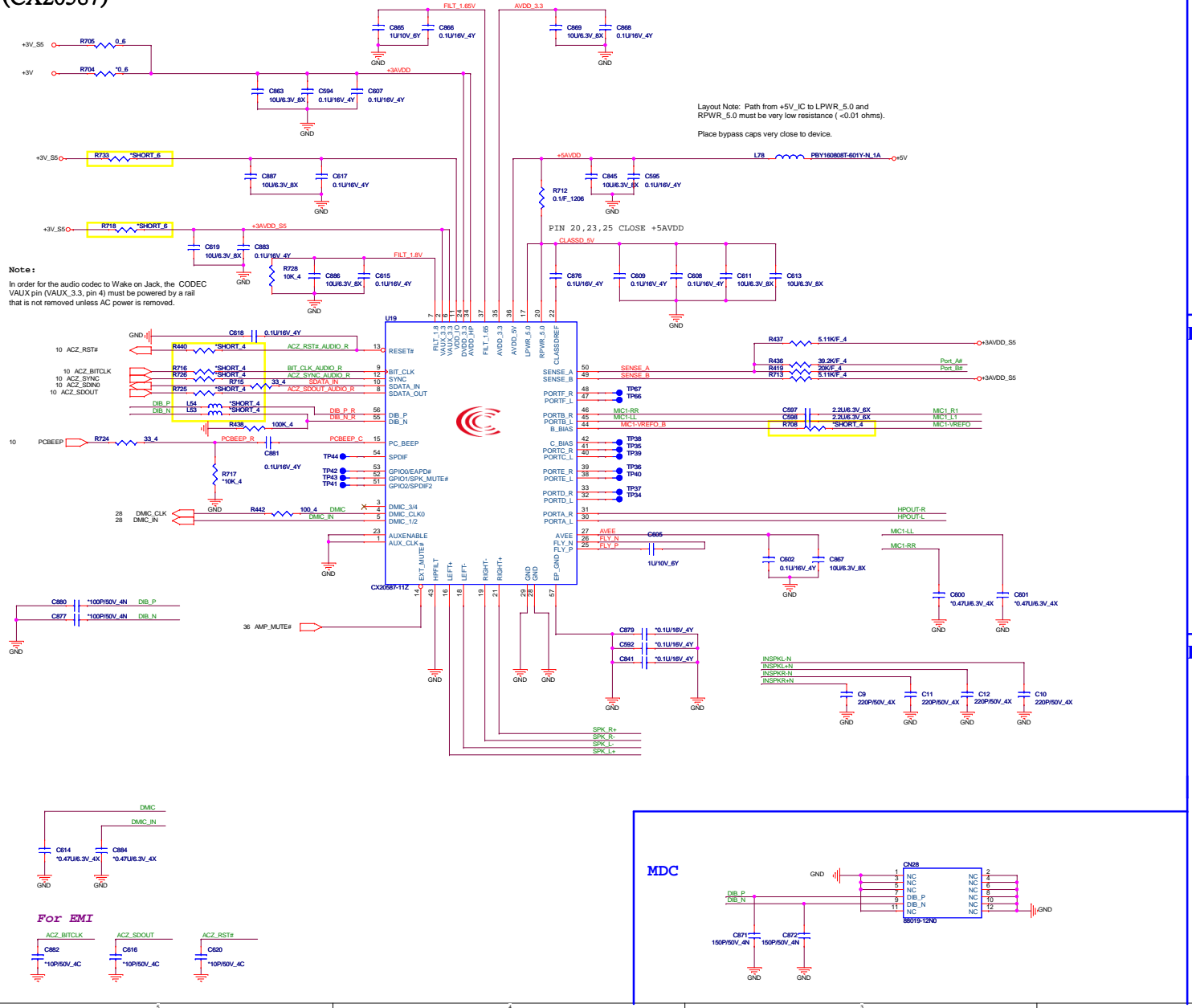


Colay with Redriver IC SATA Re-driver Bypass

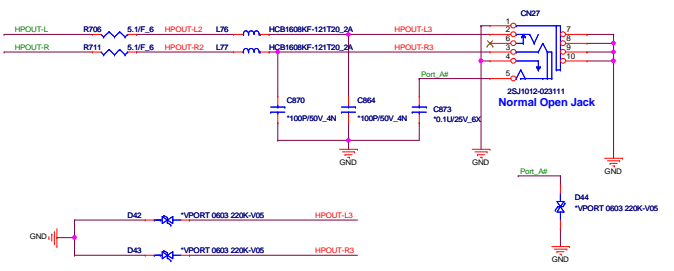
SATA_TXP0	R164	*0.4	BSATA_TXP0
SATA_TXN0	R165	*0.4	BSATA_TXN0
SATA_RXN0	R166	*0.4	BSATA_RXN0_C
SATA_RXP0	R167	*0.4	BSATA_RXP0_C

E3A

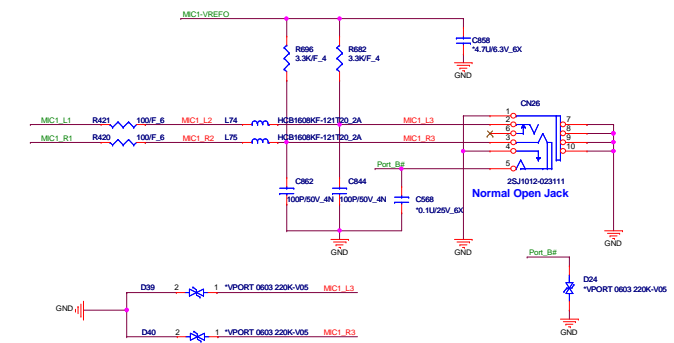
Codec  
(CX20587)



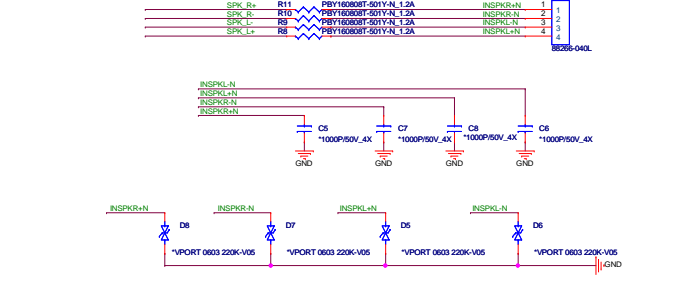
Earphone



External MIC

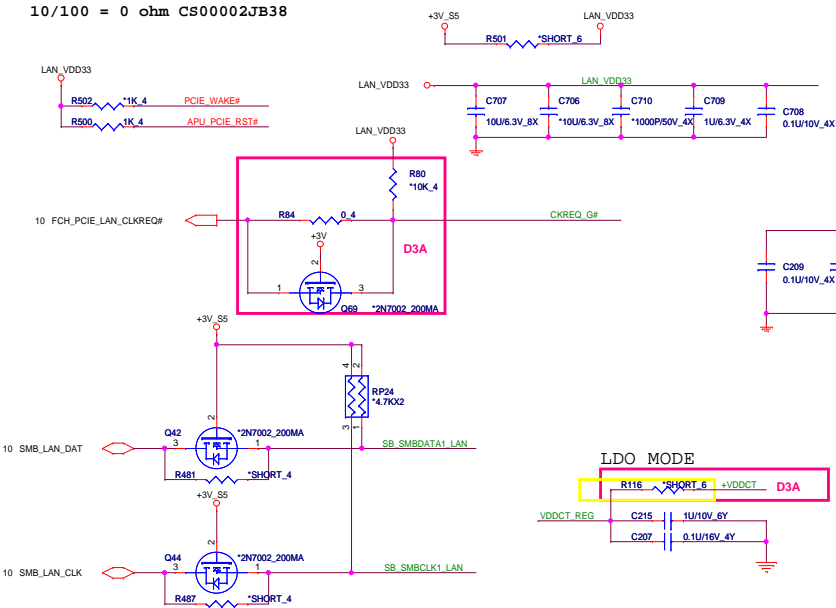


Internal Speaker

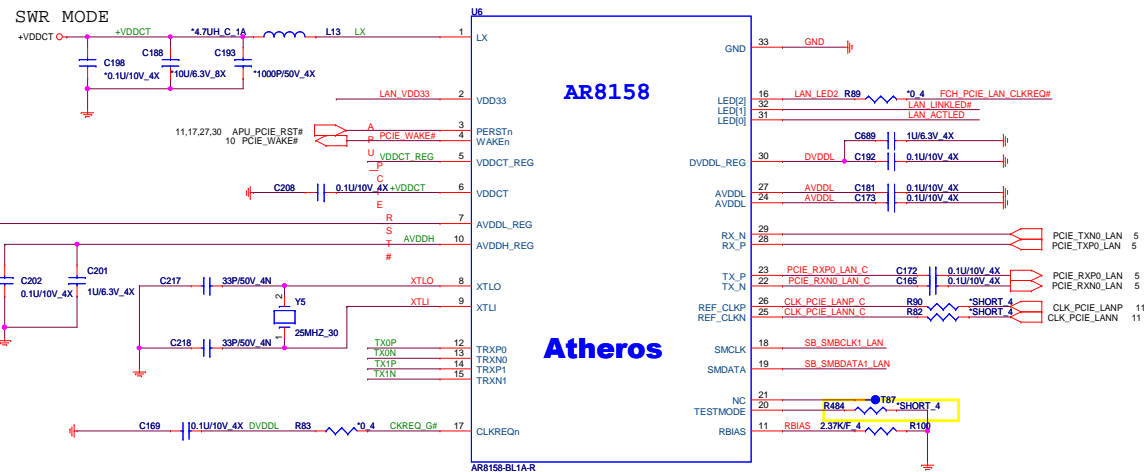
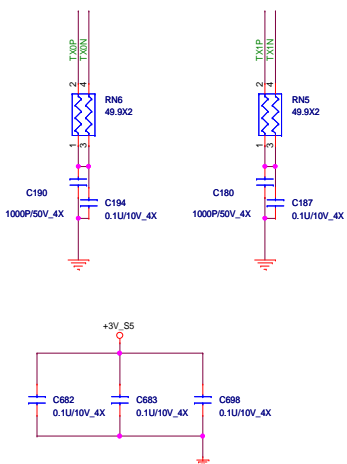


## Atheros Lan AR8158

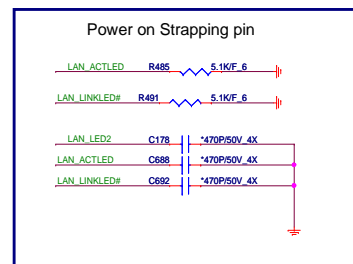
10/100 = 0 ohm CS00002JB38



PLACE NEAR LAN IC SIDE

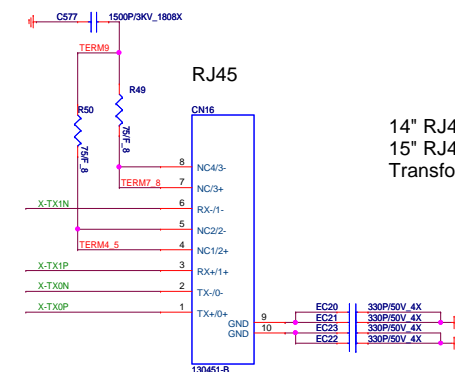
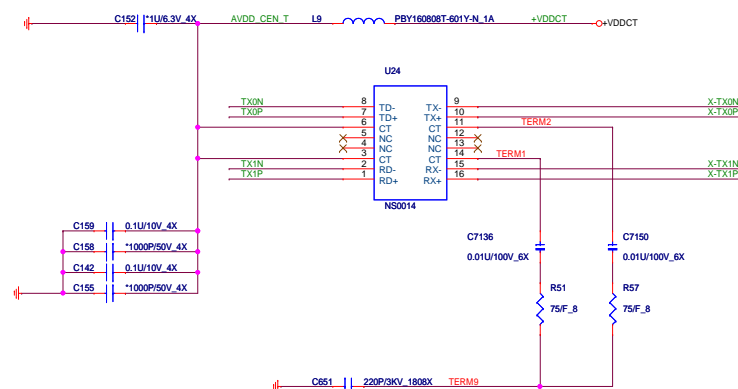


AMD 10/100: AR8158-BL1A-R = AL008158001

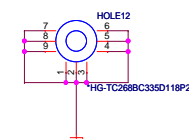


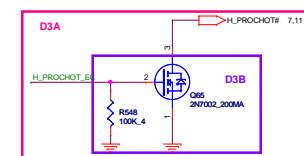
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

## TRANSFORMER



14" RJ45- DFTJ08FR164  
15" RJ45- DFTJ08FR169  
Transformer- DB0EL5LAN02



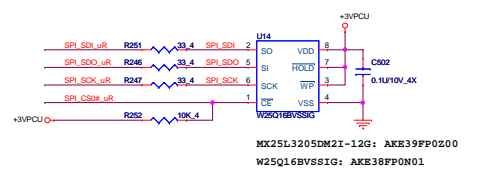
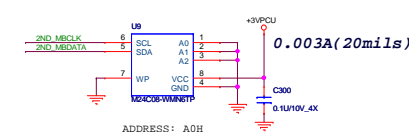


### SMBUS Table

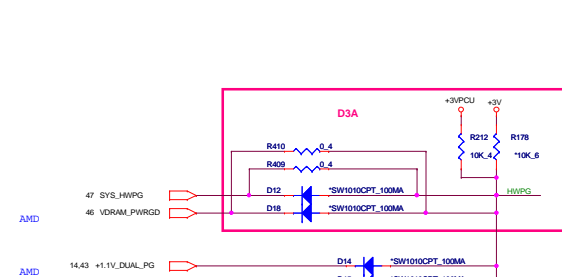
SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	ADH
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H



0.003A(20mils)

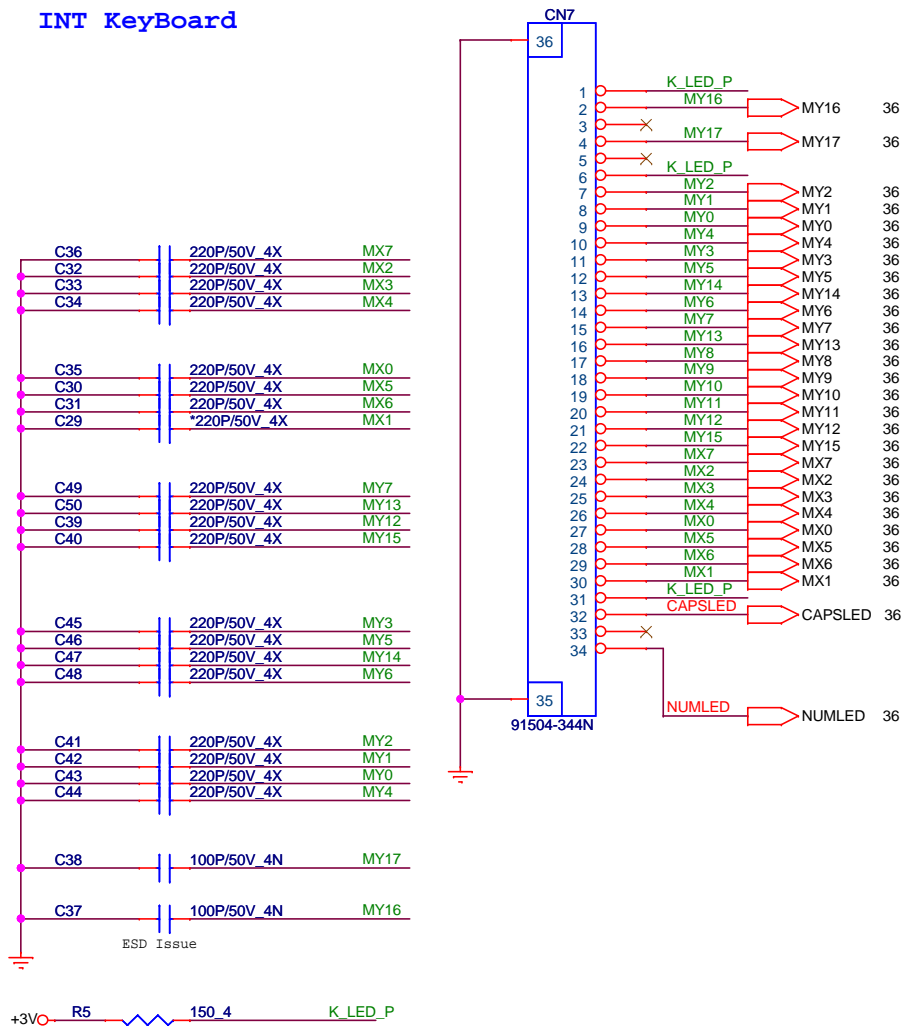


MYO R153 10K 4



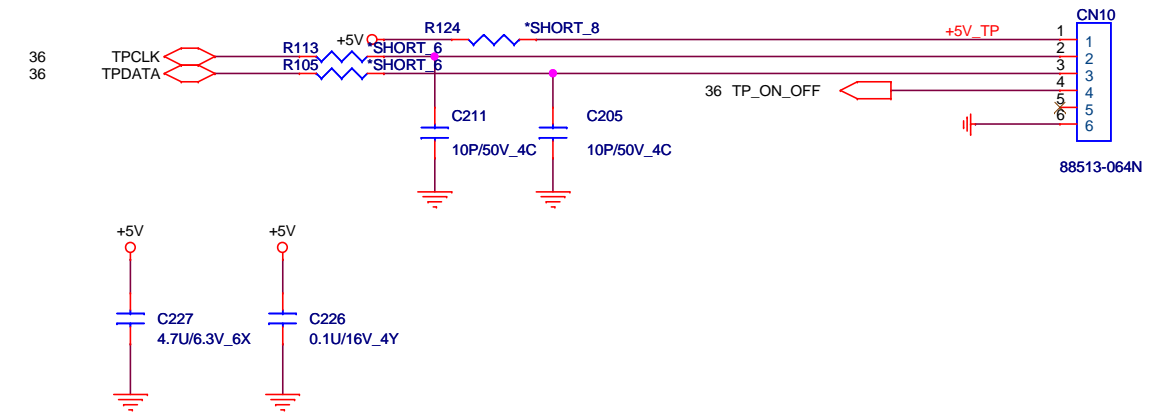
# KEY BOARD Connector

## INT KeyBoard

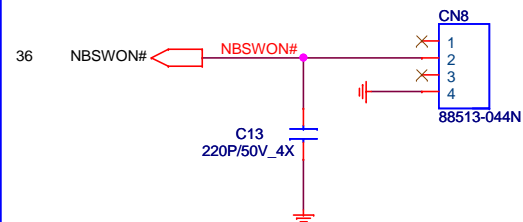


# TOUCH PAD BOARD

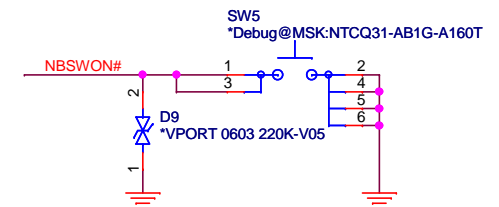
37



## Power Board (UIF)



## Power Switch (debug only)



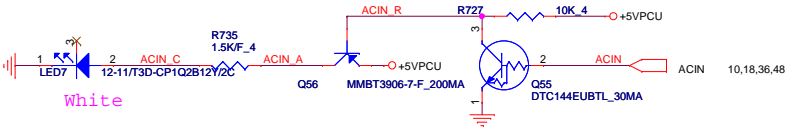
Quanta Computer Inc.

PROJECT : BLF\_BLFD

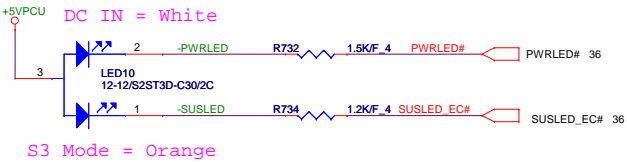
Size	Document Number	Rev
	FP/TP/KB Conn	1C
Date:	Tuesday, April 19, 2011	Sheet 37 of 53

## LED

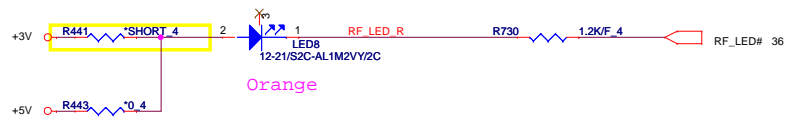
### AC-IN



### POWER



### RF LED

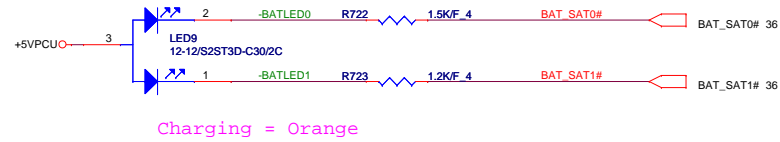


When ON, means in S0  
When BLINK, means in S3  
When OFF, means in S5

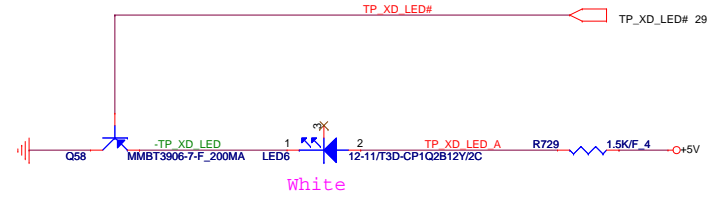
Orange

## BATTERY

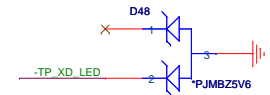
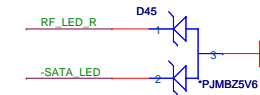
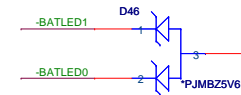
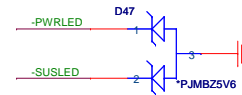
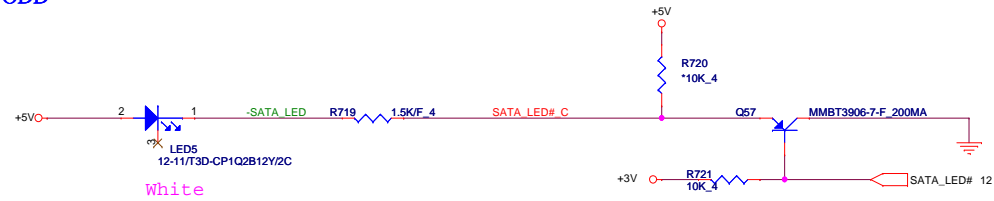
Full Charge = White



## CARDREADER



## HDD/ODD



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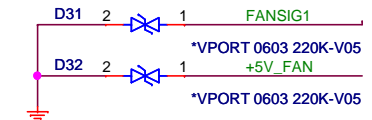
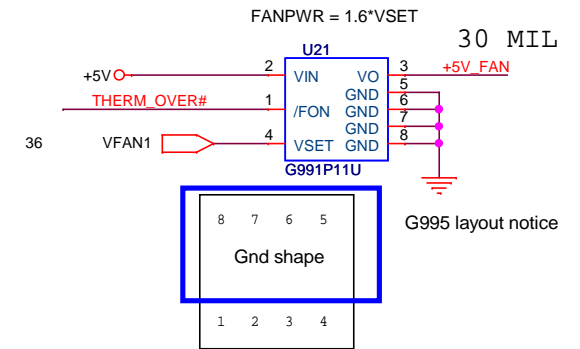
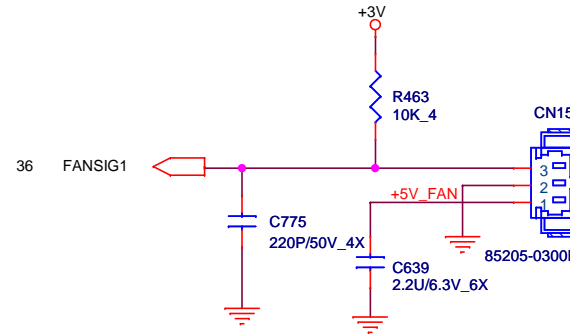
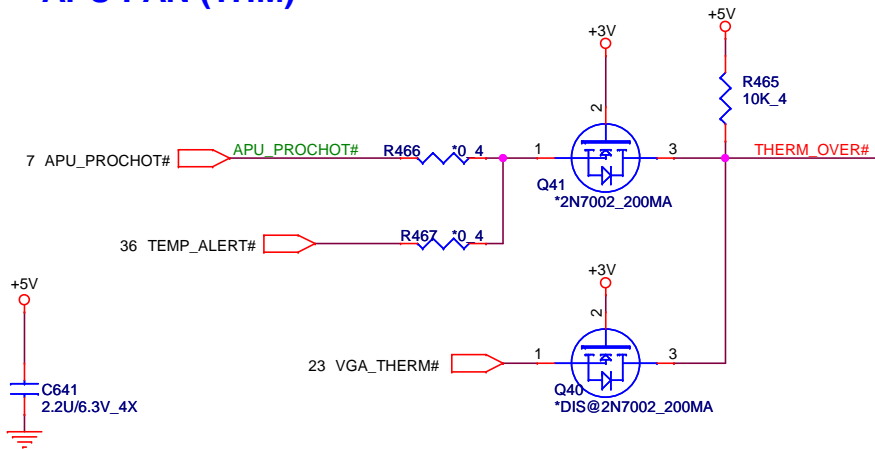
Quanta Computer Inc.

PROJECT : BLF\_BLFD

Size	Document Number	Rev
	LED	1C
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# APU FAN (THM)

39



D

D

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B

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A




**Quanta Computer Inc.**

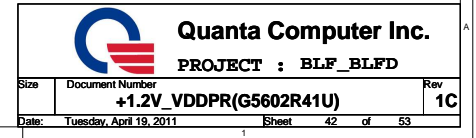
**PROJECT : BLF\_BLFD**

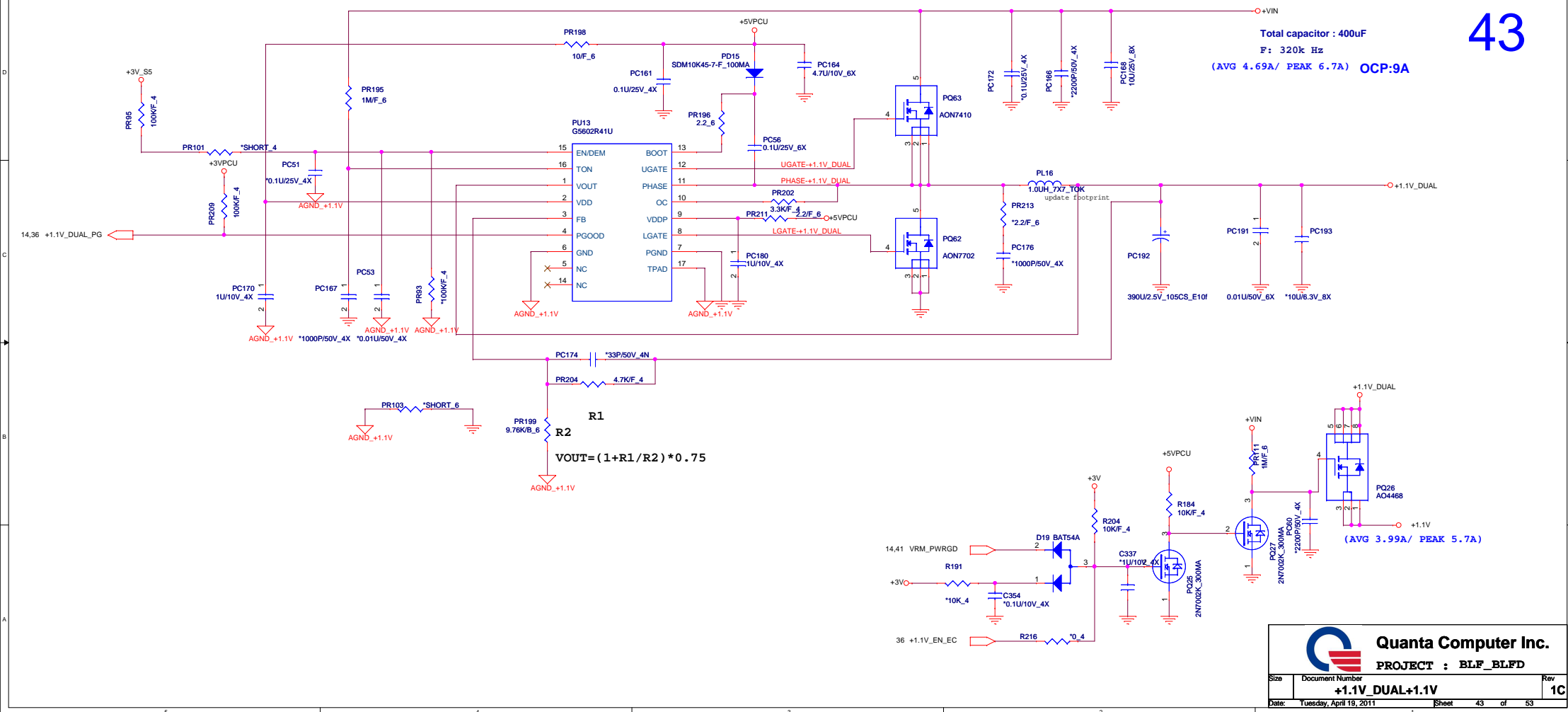
Size	Document Number	Rev
	<b>BLANK</b>	<b>1C</b>
Date:	Tuesday, April 19, 2011	Sheet 40 of 53

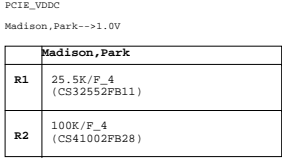
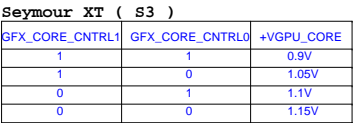


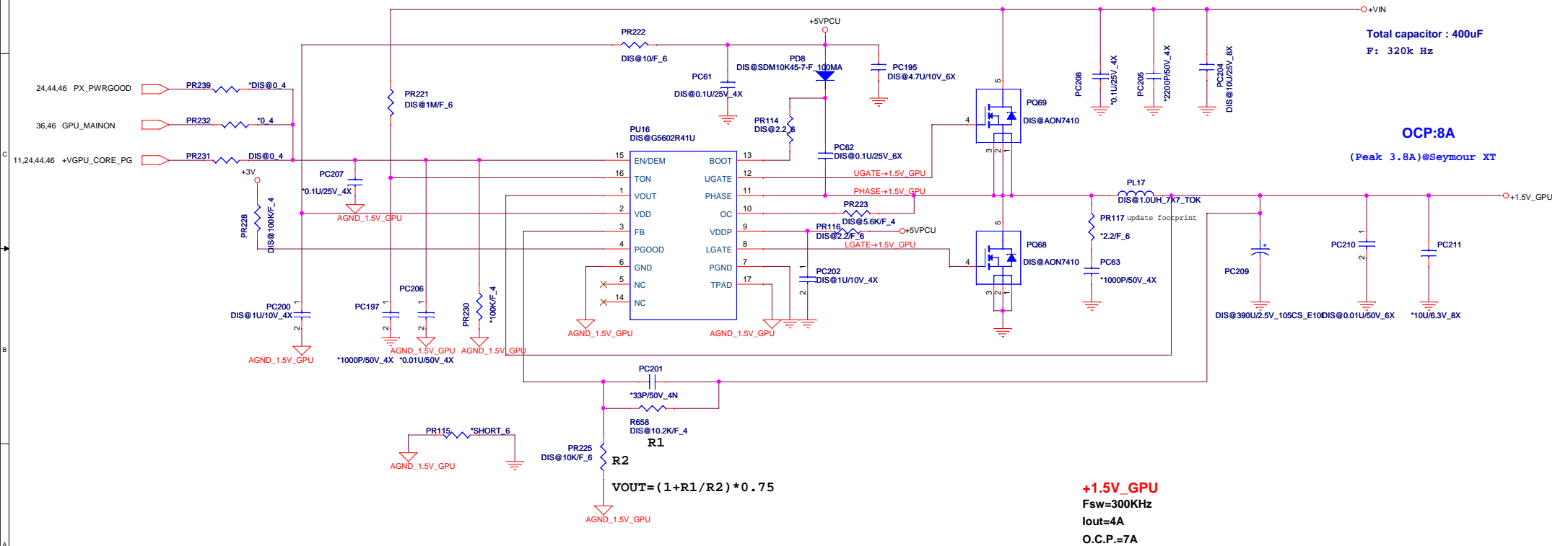


 <b>Quanta Computer Inc</b> <b>PROJECT : BLF_BLF0</b>	
Size	Document Number
	<b>CPU CORE</b>





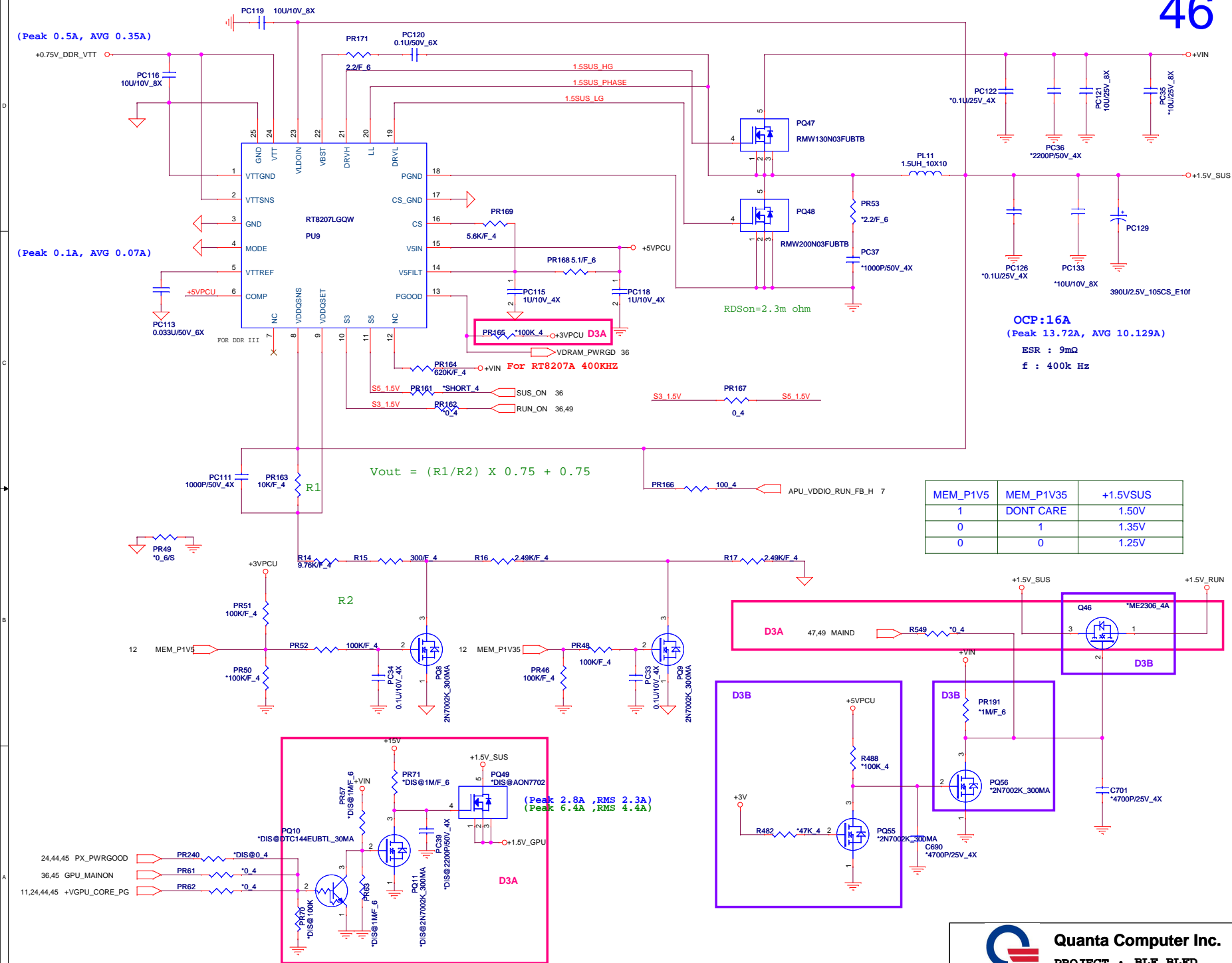


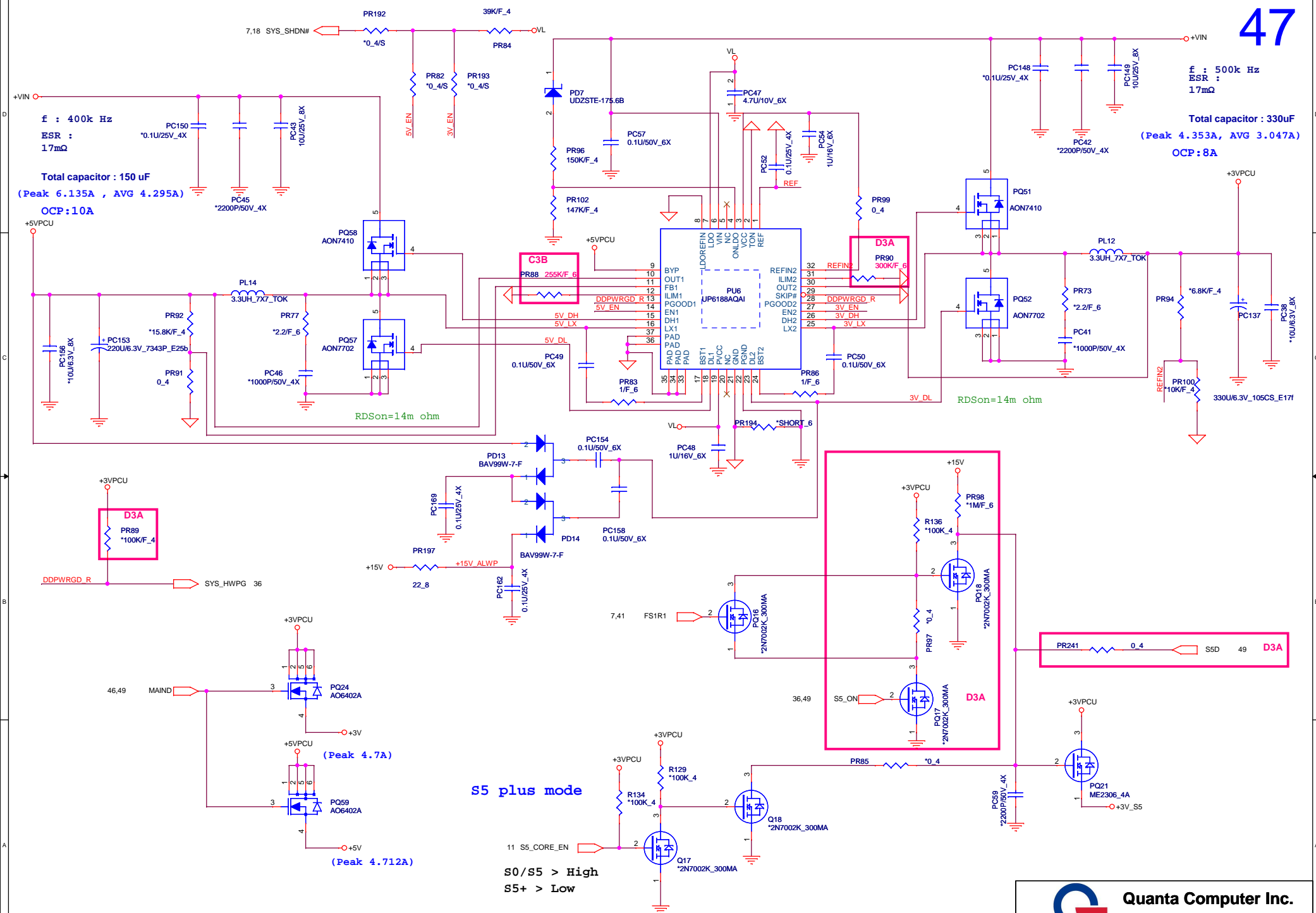


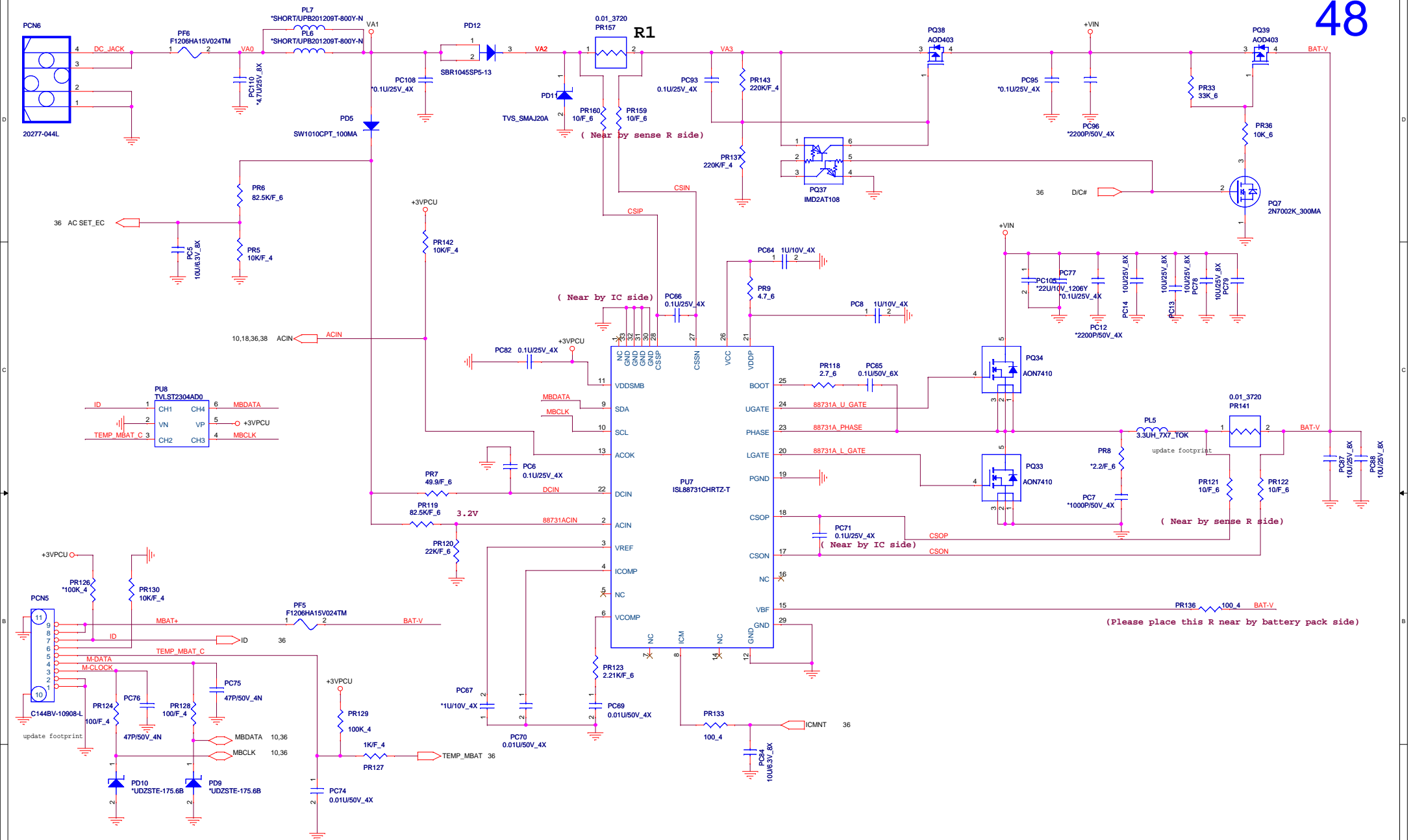
**Quanta Computer Inc.**

**PROJECT : BLF\_BLFD**

Size	Document Number	Rev
	<b>+1.5V_GPU</b>	<b>1C</b>
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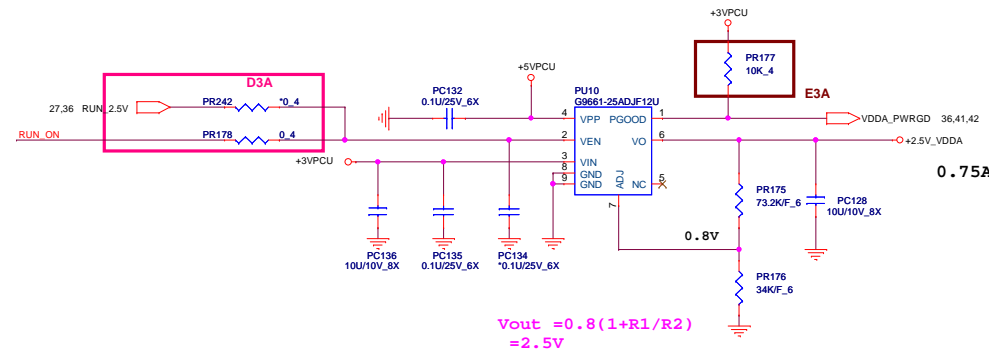
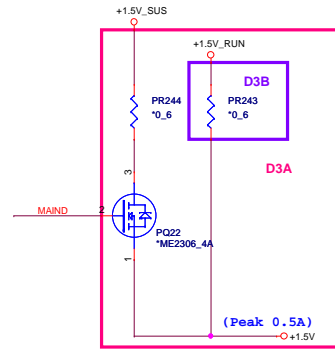


Quanta Computer Inc.

PROJECT : BLF\_BLFDD

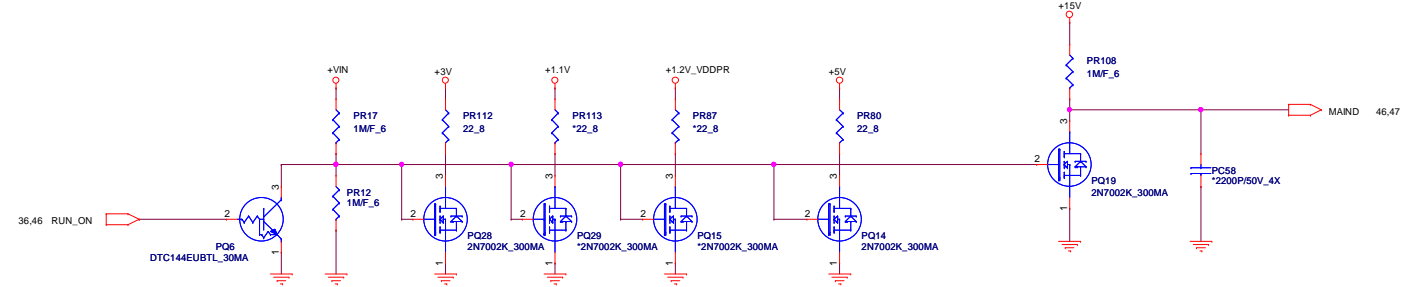
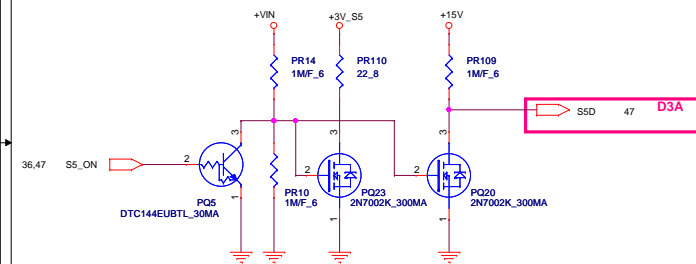
Size	Document Number	Rev
	CHARGER	1C
Date:	Tuesday, April 19, 2011	Sheet 48 of 53





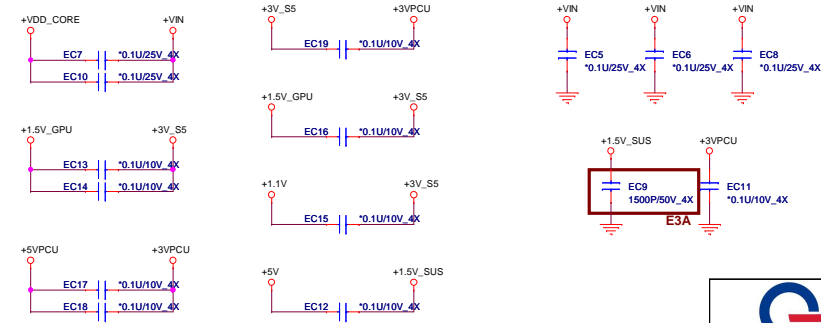
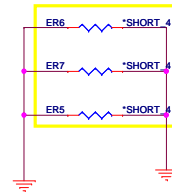
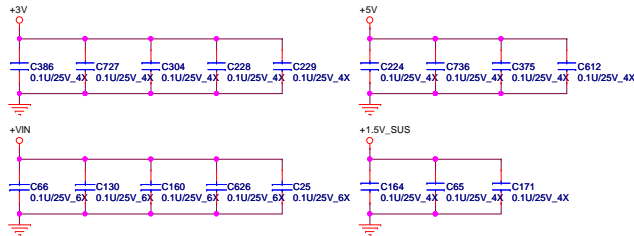
0.75A

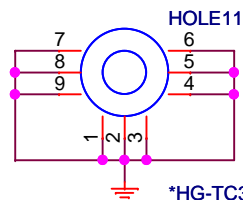
$$V_{out} = 0.8(1 + R1/R2) = 2.5V$$



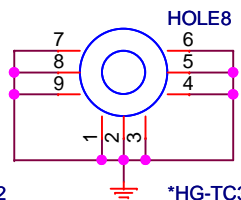
## EMI

For EMI

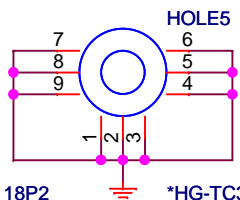




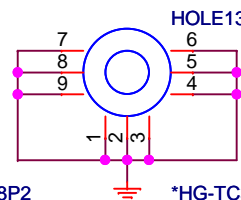
\*HG-TC335BC268D118P2



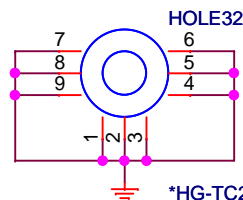
\*HG-TC335BC268D118P2



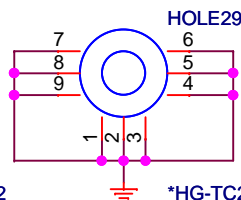
\*HG-TC335BC268D118P2



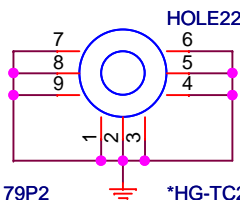
\*HG-TC335BC268D118P2



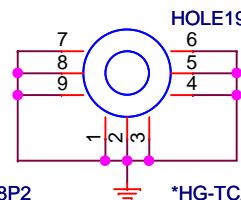
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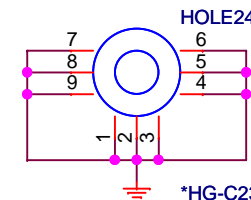
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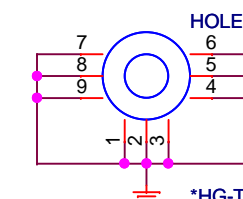
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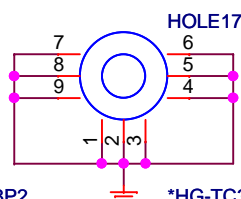
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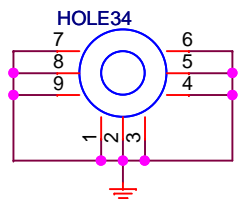
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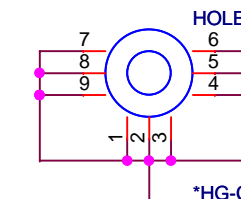
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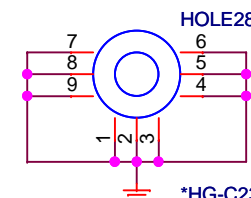
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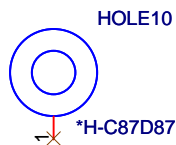
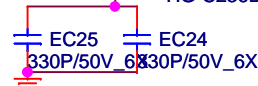
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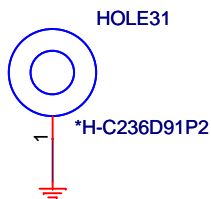
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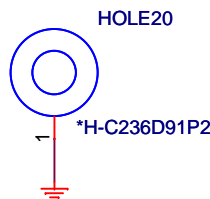
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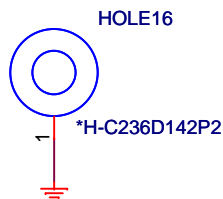
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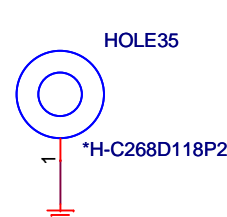
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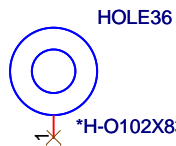
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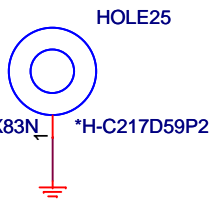
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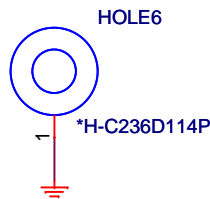
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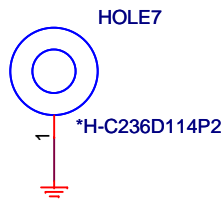
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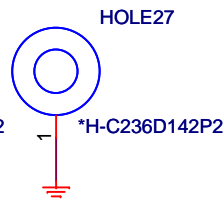
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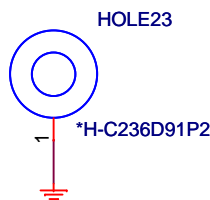
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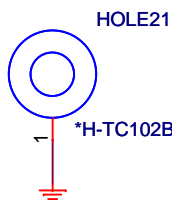
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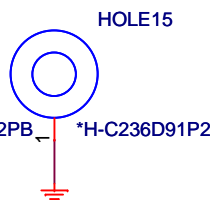
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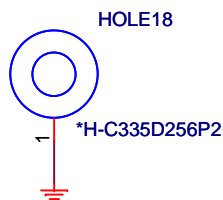
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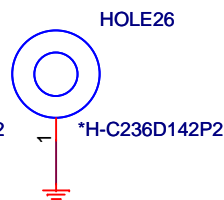
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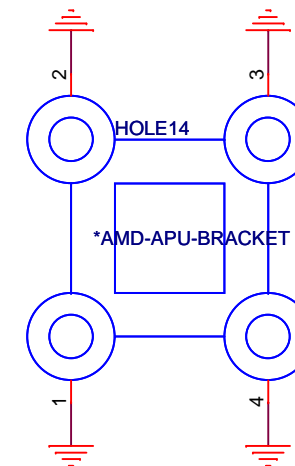
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